ESD Association Standard Practice

for the Protection of Electrostatic Discharge Susceptible Items

Standard Practice for Human Body Model (HBM) and Machine Model (MM) Alternative Test Method: Split Signal Pin – Component Level

ANSI/ESD SP5.1.2-2006

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
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FOREWORD

This standard practice defines an alternative test method to perform Human Body Model (HBM) or Machine Model (MM) component level electrostatic discharge (ESD) tests when the component or device pin count exceeds the number of ESD simulator tester channels. If an ESD simulator above 512 pins is not available, then this standard practice can be used as a guide to ESD stress components with greater than 512 pins or balls.

Since this document is a standard practice and not a standard test method, classifications of ESD sensitivity levels cannot be defined. This document references the ANSI/ESD STM5.1 (HBM) and ANSI/ESD STM5.2 (MM) test methods. Both of these documents will surpass this standard practice if there are any conflicts in testing a component.

This document does not claim to reproduce the same test results as would be achieved by an ESD simulator with greater than 512 pins. The test results will be similar, but not identical since many of the tester parasitic properties of a higher pin count simulator cannot be reproduced using a lower pin count ESD simulator. The authors of this document recommend that the user purchase and use the high pin ESD simulator that fully meets the test requirements of ANSI/ESD STM5.1 or ANSI/ESD STM5.2. If this is not possible, then this document can be used to perform HBM or MM stress testing.

This standard practice applies to both HBM and MM test methods because this alternative test method builds custom test fixture boards (TFBs) that can used by both ESD test methods. The use of these custom TFBs changes the pin combinations and not the discharge waveforms.

This standard practice was processed and approved for submittal to the Electrostatic Discharge Association (ESDA) Standards Committee by the 5.1 (HBM) Device Testing Subcommittee. The ESDA Standards Committee approved this document on September 10, 2006.

At the time this document was presented to the ESDA Standards Committee, the 5.1 (HBM) Device Testing Subcommittee had the following members:

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	Scott Ward Cypress Semiconductor	

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1.0 PURPOSE AND SCOPE

1.1 Purpose

This standard practice establishes an alternative test method to perform Human Body Model (HBM) or Machine Model (MM) component level electrostatic discharge (ESD) tests when the component or device pin count exceeds the ESD simulator tester channels. This alternative test method is limited to components with greater than 512 pins or balls. Since many of the tester parasitic properties of a higher pin count ESD simulator cannot be reproduced using a low pin count ESD simulator, the test results will be similar, but not identical. This document references ANSI/ESD STM5.1 (HBM) and ANSI/ESD STM5.2 (MM) test methods. Both of these documents will override this standard practice if there are any conflicts in testing a component. If an ESD simulator above 512 pins is not available, then this standard practice can be used as a guide to ESD stress components with greater than 512 pins or balls using a lower pin count ESD simulator.

1.2 Scope

For high pin count components (e.g., ball grid array) with a large number of signal pins, the total number of pins can be reduced by splitting the signal pins into two or more equal sets or subgroups. Special test fixture boards (TFBs) can be constructed to connect each set of signal pins to specific tester channels while floating the remaining unused signal pins. Additional TFBs can be constructed to connect each remaining set of signal pins to specific tester channels while floating the remaining unused signal pins. All power, ground and control pins on the component should be wired to each TFB.

2.0 REFERENCED PUBLICATIONS

ESD ADV1.0, Glossary of Terms[1]

ANSI/ESD STM5.1, Human Body Model (HBM) – Component Level[1]

ANSI/ESD STM5.2, Machine Model (MM) – Component Level[1]

3.0 DEFINITIONS

The following definitions are in addition to those in the ESD Glossary of Terms.

Signal Pin. Any pin that does not supply power or ground to the component.

Special Signal Pin Pairs (SSPP). Some specialized pins are connected together as a pair of pins. For example, XTAL or LVDSOUT IO pairs are differential type IO pairs.

RF PIN Pairs (RFPP). Specialized high frequency radio frequency pins that are connected together as a pair of pins.

Tester Channels. The direct communication between the ESD simulator and the pin under test (PUT) is provided by a set of relay signals or wiring paths that transfers the voltages and currents from the simulator to the PUT during the ESD test and measurement sequences.

[1] ESD Association, 7900 Turin Road, Bldg. 3, Rome, NY 13440, 315-339-6937

4.0 REQUIRED EQUIPMENT

4.1 HBM / MM ESD Tester

An acceptable ESD tester is composed of equipment meeting the requirements of ANSI/ESD STM5.1 and ANSI/ESD STM5.2. See Figure 1.

4.2 Waveform Verification Equipment

Equipment capable of verifying the pulse waveforms defined in ANSI/ESD STM5.1 and ANSI/ESD STM5.2. See documents for further information.

4.3 Custom Test Fixture Board

A TFB may be required to reduce the number of tester channels needed to perform stress testing. If required, custom TFBs that are specific to a particular component may be designed and constructed.

4.3.1 This procedure requires the design and building of custom TFBs that may be specific to a particular component. Annex A shows a process flow that can be used to help identify the need for a custom TFB.

4.3.2 To determine how many custom TFBs are required, compare the component pin count to the number of tester channels available. Subtract the total number of non-signal (power and ground) pins from the total number of tester channels. Divide this number into the total number of signal pins and round up to the largest whole number. (See Annex B for further information.)

4.3.3 Select and wire a set or subgroup of signal pins to each TFB, along with all component supply, ground and control pins.

4.3.4 Each set or subgroup of signal pins should represent the different signal pin types used on the component. The selection should not be arbitrary. A minimum of at least two signal pins from each unique signal pin group should be included on each custom TFB. Signal pins that are related by shared function or circuitry (e.g., SSPP or RF pairs) must be electrically wired on the same TFB.

4.3.5 Typically, two custom TFBs can be constructed allowing the stressing of all component pins. In this case, each custom TFB will wire approximately 50% of all component signal pins.

4.3.6 If more than two TFBs are necessary, then each TFB should attempt to wire an equal number of component signal pins.

NOTE 1: It is recommended that all supply pins, ground pins, control pins and signal pin sets be wired to each custom TFB using the same tester channels. This will allow for a similar test program to be used for each custom TFB.

NOTE 2: Ideally a third TFB that wires all of the signal pins and no supply pins could be built. This additional board would allow the stressing of a single signal pin while grounding all other signal pins. This document leaves the construction of this third TFB optional and not required.

5.0 EQUIPMENT AND WAVEFORM REQUIREMENTS

5.1 Equipment Calibration

All equipment used to evaluate the tester shall be periodically calibrated in accordance with the manufacturer's recommendation. See ANSI/ESD STM5.1 and ANSI/ESD STM5.2 for further information.

5.2 Tester Qualification and Re-qualification

HBM/MM ESD tester initial qualification is completed in accordance with ANSI/ESD STM5.1 and ANSI/ESD STM5.2.

5.3 Tester Waveform Records

Tester waveform records are to be maintained in compliance to ANSI/ESD STM5.1 and ANSI/ESD STM5.2.

6.0 QUALIFICATION AND VERIFICATION PROCEDURES

6.1 ESD Tester and Test Fixture Board Qualification Procedure

HBM/MM ESD tester qualification shall ensure waveform integrity of the peak current into a short (Ips). See ANSI/ESD STM5.1 and ANSI/ESD STM5.2 for further information.

6.2 Waveform Verification Procedure

To verify the HBM/MM waveform verification procedures, see ANSI/ESD STM5.1 and ANSI/ESD STM5.2 for further information.

6.3 Waveform Verification Following Servicing

Verify the waveforms meet all parameters specified after any repairs or servicing of the tester in compliance with ANSI/ESD STM5.1 and ANSI/ESD STM5.2.

7.0 ESD TESTING REQUIREMENTS AND PROCEDURES

7.1 Test Requirements

7.1.1 Handling of Components

Use ESD damage prevention procedures when handling components before, during, and after testing.

7.1.2 Required Waveform Check

Verify waveform integrity described in ANSI/ESD STM5.1, Section 8 (ESDS Testing Requirements and Procedures); and ANSI/ESD STM5.2, Section 7 (Qualification and Verification Procedures).

7.1.3 High Voltage Discharge Path Check

Verify high voltage discharge path described in ANSI/ESD STM5.1, Section 8 (ESDS Testing Requirements and Procedures); and ANSI/ESD STM5.2, Section 7 (Qualification and Verification Procedures).

7.1.4 Component static and dynamic tests

To determine whether components have failed, perform static and dynamic testing to all data sheet parameters before and after ESD testing. Pin leakage current may only be used as guides in determining the component ESD withstand voltage. It is not sufficient, especially for complex integrated circuits, to use pin leakage as the only criterion for component failure.

7.1.5 Modified Pin Combinations

The pin combinations to be used for ESD stressing of all components are given in Table 1. Pin combination (n) is the total number of pin combinations. This varies from component to component depending on the number of power pin groups with the same name, Vps(i) in Table 1.

For those components with more pins than the ESD simulator tester channels, custom TFBs can be designed and constructed to split the total number of component signal pins into two or more sets or subgroups. All supply, ground and control pins must be wired to each TFB. See Annex B and Table 4 for an example of the modified test pin combinations.

Table 1. Modified Pin Combinations for HBM and MM Testing

Pin Combination Set	Connect Individually to Terminal A	Connect to Terminal B (Ground)	Floating Pins (Unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	Vps(1) [First power pin(s)]	All pins except pin under test (PUT) and Vps(1) [First power pin]
2	All pins one at a time, except the pin(s) connected to Terminal B	Vps(2) [Second power pin(s)]	All pins except PUT and Vps(2) [Second power pin]
i	All pins one at a time, except the pin(s) connected to Terminal B	Vps(i) [ith power pin(s)] [1,2, ...i]	All pins except PUT and Vps(i)
n-1	All pins one at a time, except the pin(s) connected to Terminal B	Vps(n-1)	All pins except PUT and Vps(n-1)
n = (# of TFB) x (# of signal pin sets)	All non-Vps(i) pins one at a time for each signal pin set on each TFB (repeat until all signal pin sets are stressed)	All other non-Vps(i) pins, except the pin connected to Terminal A	All Vps(i) pins and any signal pin not wired on the TFB being used

7.2 ESD Stress Testing Procedure

Perform ESD stress testing at room temperature in accordance with the procedure below. It is permissible to use any voltage level in Table 2 (HBM) or Table 3 (MM) as the starting stress level. Three new components may be used at each voltage level or pin combination if desired. This will eliminate any step stress hardening effects and reduce the possibility of early failure due to cumulative stress on power pins. However, if a single set of three components is stressed at each level, then to avoid missing possible ESD vulnerability windows, it is recommended not to miss any stress step.

Table 2. HBM ESD Stress Levels

Stress Level	Equivalent Charging (±) Voltage Vp (volt)
1	250
2	500
3	1000
4	2000
5	4000
6	8000 (optional)

Table 3. MM ESD Stress Levels

Stress Level	Equivalent Charging (±) Voltage Vp (volt)
1	100
2	200
3	400

NOTE 3: A component may pass at 4000 volts but fail at 2000 volts; this is called a component fail window. To avoid this fail window, it is recommended that components be tested at each level defined in Table 2 (HBM) or Table 3 (MM).

Use the following procedure to ESD stress the components:

7.2.1 Test a minimum of three samples of the component to all specified static and dynamic data sheet parameters.

7.2.2 Place one of the custom TFBs on the ESD simulator and set up the appropriate test program for that custom TFB.

7.2.3 Determine the starting stress voltage level from Table 2 (HBM) or Table 3 (MM). Select the first pin combination to be tested as stated in Section 7.1.5 and Table 1.

7.2.4 For HBM testing, apply one positive and one negative pulse to the component. Allow at least a 0.3 second interval between pulses. Repeat this process using all other pin combinations specified in Section 7.1.5 and Table 1.

7.2.5 For MM testing, apply three positive and three negative pulses to the component. Allow at least a 1.0 second interval between pulses. Repeat this process using all other pin combinations specified in Section 7.1.5 and Table 1.

NOTE 4: One pulse per polarity is used only for ANSI/ESD STM5.1 and is not permitted for ANSI/ESD STM5.2.

7.2.6 After all pins have been stressed, place the second or additional TFBs and set up the appropriate test program for that custom TFB. Repeat steps 7.2.3 through 7.2.5 for each custom TFB.

7.2.7 Test the components to full static and dynamic data sheet parameters and record the results for each component. Parametric and functional testing shall be performed at room temperature. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

7.2.8 If all three components pass the specified data sheet parameters, repeat steps 7.2.3 through 7.2.7, using the next higher stress level of Table 2 (HBM) or Table 3 (MM). Three new components may be used at each voltage level or pin combination if desired.

7.2.9 If one or more components fail, repeat the ESD stress test using three new components starting at the next lower stress level. If the components continue to fail, decrease the stress voltage until level 1 is reached in Table 2 (HBM) or Table 3 (MM). If any additional failures are observed at level 1, stop all testing at this level.

8.0 FAILURE CRITERIA

A component is considered an ESD failure if it fails the data sheet parameters as specified in Section 7.1.4.

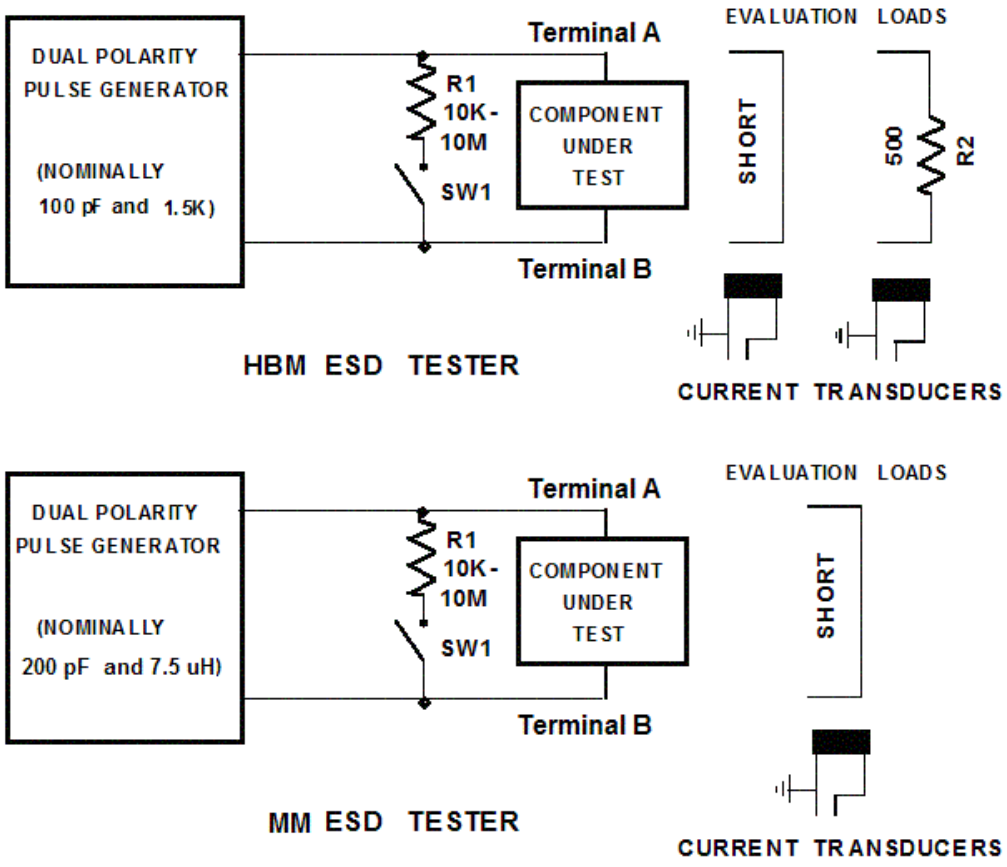


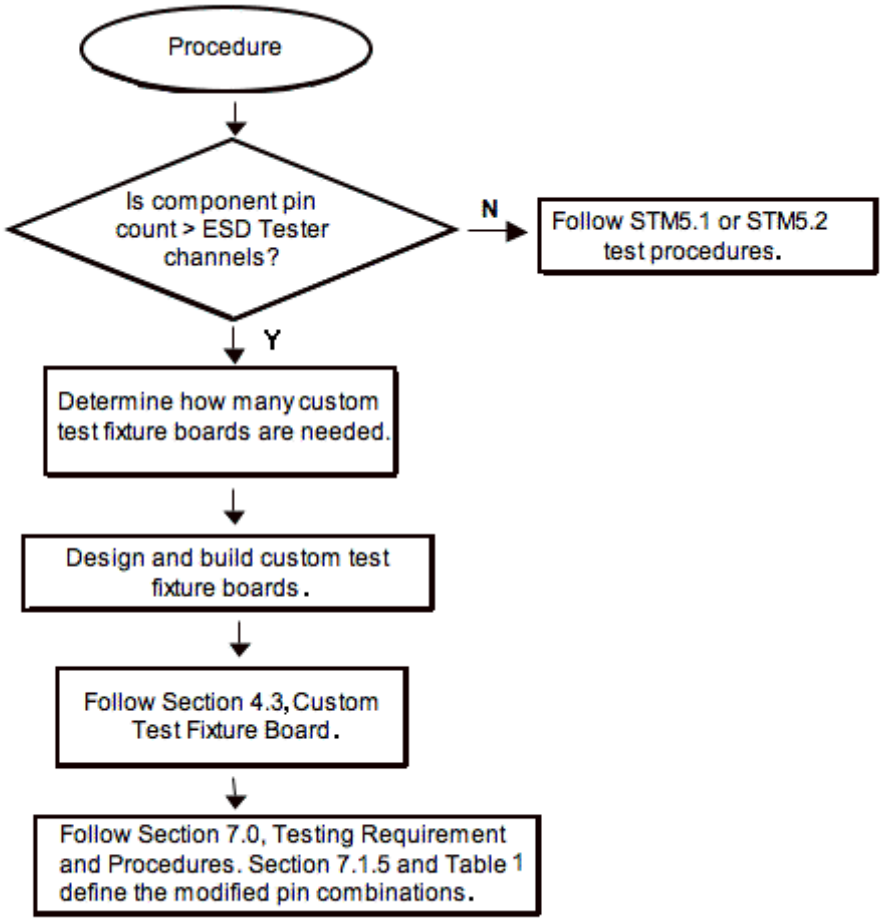
Figure 1: Typical Equivalent Stress Test Circuits

Requirements:

1. See ANSI/ESD STM5.1 for detailed HBM requirements.
2. See ANSI/ESD STM5.2 for detailed MM requirements.

(This annex is not part of ANSI/ESD SP5.1.2-2006)

ANNEX A – SPLIT SIGNAL PIN ATM CUSTOM TEST FIXTURE BOARD PROCEDURE FLOW



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ANNEX B – EXAMPLE OF SPLIT SIGNAL PIN METHOD

Given an ESD test simulator with 512 pins (or tester channels), a component with 560 pins or balls would require custom test fixture boards (TFBs) as shown in Figure 2. Figure 2(a) defines the 560 pin component. Following the equation defined in Section 4.3 and shown in Figure 2(b), the 560 pin component could be stressed on a 512 pin tester by using 2 custom TFBs. Figure 2(c) shows how the component pins would be divided among the custom TFBs. Table 4 illustrates the modified test pin combinations to be used with the custom TFBs.

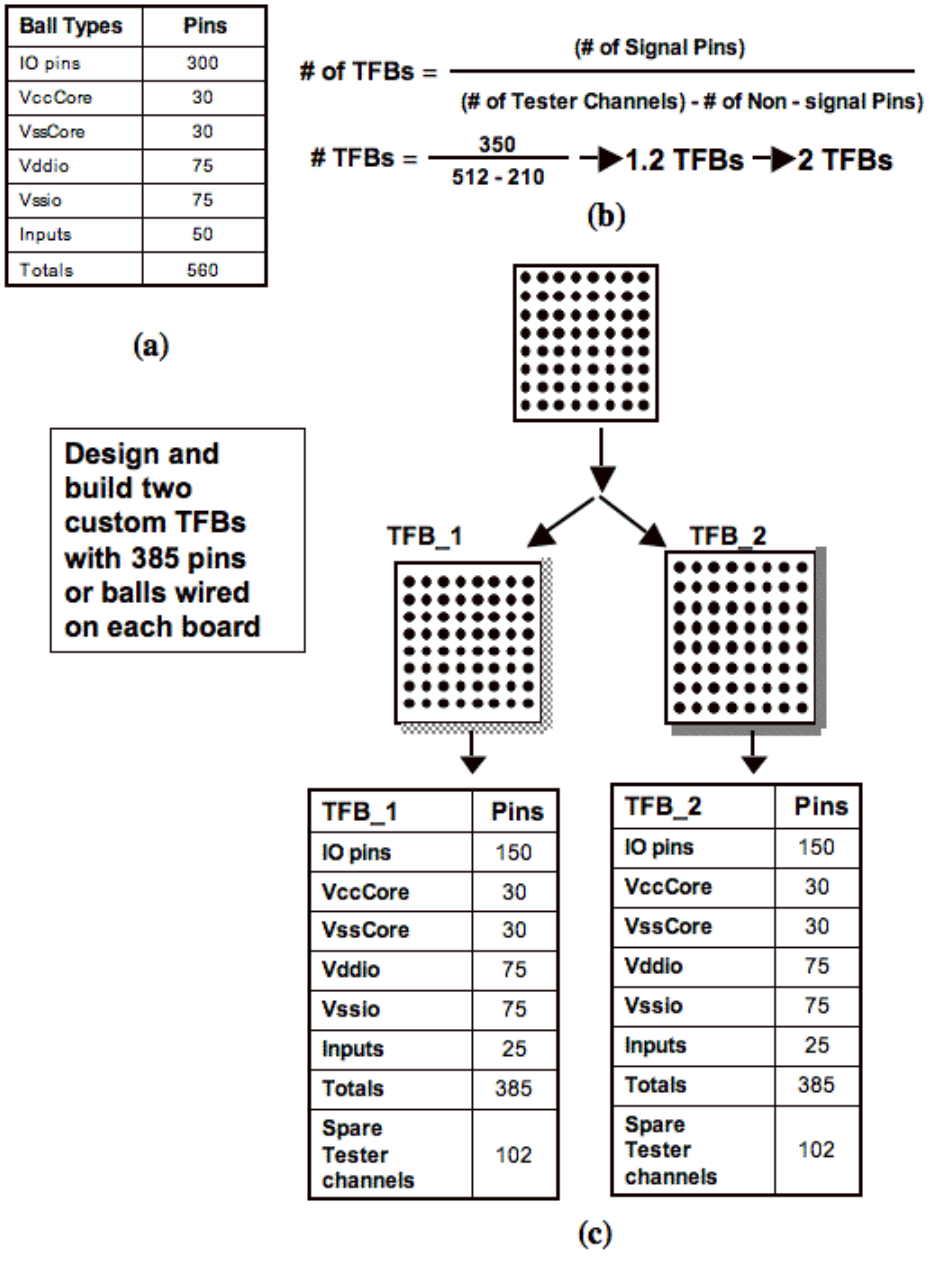

Figure 2: Example of Split Signal Pin Method

NOTE 5: The 300 IO pins are split into two equal groups of 150 pins. Each set of IO pins is wired on each custom TFB to separate tester channels. All supply, ground and control pins are wired on each custom TFB.

Table 4. Example of HBM and MM Modified Test Pin Combinations for Multiple Custom TFBs

Custom TFB No.	Pin Combination Set	Connect Individually to Terminal A (all pins one at a time)	Connect to Terminal B (Ground)	Floating Pins (Unconnected)
1	1	Signal Pin Set (1), VssCore, VddIO, and VssIO	VccCore	Signal Pin Set (2) and all pins except pin under test (PUT) and VccCore
	2	Signal Pin Set (1), VccCore, VddIO, and VssIO	VssCore	Signal Pin Set (2) and all pins except PUT and VssCore
	3	Signal Pin Set (1), VccCore, VssCore, and VssIO	VddIO	Signal Pin Set (2) and all pins except PUT and VddIO
	4	Signal Pin Set (1), VccCore, VssCore, and VddIO	VssIO	Signal Pin Set (2) and all pins except PUT and VssIO
	5	Signal Pin Set (1)	Signal Pin Set (1)	Signal Pin Set (2), VccCore, VssCore, VddIO, and VssIO
2	6	Signal Pin Set (2), VssCore, VddIO, and VssIO	VccCore	Signal Pin Set (1) and all pins except pin under test (PUT) and VccCore
	7	Signal Pin Set (2), VccCore, VddIO, and VssIO	VssCore	Signal Pin Set (1) and all pins except PUT and VssCore
	8	Signal Pin Set (2), VccCore, VssCore, and VssIO	VddIO	Signal Pin Set (1) and all pins except PUT and VddIO
	9	Signal Pin Set (2), VccCore, VssCore, and VddIO	VssIO	Signal Pin Set (1) and all pins except PUT and VssIO
	10	Signal Pin Set (2)	Signal Pin Set (2)	Signal Pin Set (1), VccCore, VssCore, VddIO, and VssIO

(This annex is not part of ANSI/ESD SP5.1.2-2006)

ANNEX C – BIBLIOGRAPHY

MIL-STD-883D: Test Methods and Procedures for Microelectronics: Method 3015.7 Electrostatic Discharge Sensitivity Classification.

MIL-STD-750C Notice 4: Test Methods for Semiconductor Devices: Method 1020: Electrostatic Discharge Sensitivity Classification.