ESD Association Standard Practice

for the Protection of Electrostatic Discharge Susceptible Items

Standard Practice for Human Body Model (HBM) and Machine Model (MM) Alternative Test Method: Supply Pin Ganging Component Level

ANSI/ESD SP5.1.1-2006

Electrostatic Discharge Association
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Rome, NY 13440

An American National Standard
Approved October 13, 2006

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Published by:

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

Printed in the United States of America

ISBN: 1-58537-122-X

(This foreword is not part of ANSI/ESD SP5.1.1-2006)

FOREWORD

This standard practice defines an alternative test method to perform Human Body Model (HBM) or Machine Model (MM) component level electrostatic discharge (ESD) tests when the component or device pin count exceeds the number of ESD simulator tester channels. If an ESD simulator above 512 pins is not available, then this standard practice can be used as a guide to ESD stress components with greater than 512 pins or balls.

Since this document is a standard practice and not a standard test method, classifications of ESD sensitivity levels cannot be defined. This document references the ANSI/ESD STM5.1 (HBM) and ANSI/ESD STM5.2 (MM) test methods. Both of these documents will surpass this standard practice if there are any conflicts in testing a component.

This standard practice does not claim to reproduce the same test results as would be achieved by an ESD simulator with greater than 512 pins. The test results will be similar but not identical, since many of the tester parasitic properties of a higher pin count simulator cannot be reproduced using a lower pin count ESD simulator. The authors of this document recommend that the user purchase and use the high-pin ESD simulator that fully meets the test requirements of ANSI/ESD STM5.1 or ANSI/ESD STM5.2. If this is not possible, then this standard practice can be used to perform HBM or MM stress testing.

This standard practice applies to both HBM and MM test methods because this alternative test method builds custom test fixture boards that can used by both ESD test methods. The use of these custom test fixture boards changes the pin combinations and modifies the discharge waveforms.

This standard practice was processed and approved for submittal to the Electrostatic Discharge Association (ESDA) Standards Committee by the 5.1 (HBM) Device Testing Subcommittee. The ESDA Standards Committee approved this document on September 10, 2006.

At the time this document was presented to the ESDA Standards Committee, the 5.1 (HBM) Device Testing Subcommittee had the following members:

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1.0 PURPOSE AND SCOPE

1.1 Purpose

This standard practice establishes an alternative test method to perform Human Body Model (HBM) or Machine Model (MM) component level electrostatic discharge (ESD) tests when the component or device pin count exceeds the ESD simulator tester channels. This alternative test method is limited to components with greater than 512 pins or balls. Since many of the tester parasitic properties of a higher pin count ESD simulator cannot be reproduced using a low pin count ESD simulator, the test results will be similar, but not identical. This document references ANSI/ESD STM5.1 (HBM) and ANSI/ESD STM5.2 (MM) test methods. Both of these documents will override this standard practice if there are any conflicts in testing a component. If an ESD simulator above 512 pins is not available, then this standard practice can be used as a guide to ESD stress components with greater than 512 pins or balls using a lower pin count ESD simulator.

1.2 Scope

For those components (e.g., ball grid array) that interconnect different power leads through common, low-resistance power and ground planes in the package, the number of power and ground leads can be reduced by ganging or grouping supply pins together on a custom test fixture board. A minimum number of power supply pins (i.e., power or ground) should be ganged to bring the total number of tester channels used equal to the number of tester channels available on the tester.

2.0 REFERENCED PUBLICATIONS

ESD ADV1.0, Glossary of Terms[1]

ANSI/ESD STM5.1, Human Body Model (HBM) – Component Level[1]

ANSI/ESD STM5.2, Machine Model (MM) – Component Level[1]

3.0 DEFINITIONS

The following definitions are in addition to those in the ESD Glossary of Terms:

Supply Pins. Any set of like-named power supply or ground pins or balls (e.g., Vcc, Vss, Vdd, Analog Gnd, Digital Gnd, etc.) that are metallically connected within the chip or the package. These groups are identified as Vps(i) in Section 8.1.5 of ANSI/ESD STM5.1 and Section 8.5 of ANSI/ESD STM5.2.

Tester Channel Pin. An electrical signal pin built into an ESD simulator that electrically connects the high voltage (HV), ground or floating voltage potentials from the ESD simulator to either a single pin or a group of pins placed on the test fixture board. For example, a 512-pin ESD simulator has 512 tester channel pins.

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4.0 REQUIRED EQUIPMENT

4.1 HBM / MM ESD Tester

An acceptable ESD tester is composed of equipment meeting the requirements of ANSI/ESD STM5.1 and ANSI/ESD STM5.2. See Figure 1.

4.2 Waveform Verification Equipment

Equipment capable of verifying the pulse waveforms defined in ANSI/ESD STM5.1 and ANSI/ESD STM5.2. See documents for further information.

4.3 Custom Test Fixture Board (TFB)

A custom socket card or board designed to gang power or ground pins to reduce the number of test channel pins needed to test the device under test (DUT).

4.3.1 This procedure requires the design and building of a custom test fixture board that may be specific to a particular component. The ganged pins are hard wired into groups on the custom test fixture board when the board is built.

4.3.2 Gang together the minimum number of power or ground pins required to bring the total number of pins equal to the number of tester channels available. Individual power and ground pins that connect directly from the package to the silicon cannot be ganged together since they are not shorted to a power or ground plane in the package. See an example of this power supply ganging technique in Annex A.

NOTE 1: Shorting pins together on the test fixture board will modify the waveforms. See NOTE 5 for more information.

4.3.3 For each ganged power supply group, one pin will be brought out on the board and will connect to the tester during zapping. See Annex A.

5.0 EQUIPMENT AND WAVEFORM REQUIREMENTS

5.1 Equipment Calibration

All equipment used to evaluate the tester should be periodically calibrated in accordance with the manufacturer's recommendation. See ANSI/ESD STM5.1 and ANSI/ESD STM5.2 for further information.

5.2 Tester Qualification and Re-qualification

HBM/MM ESD tester initial qualification is completed in accordance ANSI/ESD STM5.1 and ANSI/ESD STM5.2.

5.3. Tester Waveform Records

Tester waveform records are maintained in compliance to ANSI/ESD STM5.1 and ANSI/ESD STM5.2.

6.0 QUALIFICATION AND VERIFICATION PROCEDURES

6.1 ESD Tester and Test Fixture Board Qualification Procedure

HBM/MM ESD tester qualification shall ensure waveform integrity of the peak current into a short (Ips). See ANSI/ESD STM5.1 and ANSI/ESD STM5.2 for further information.

6.2 Waveform Verification Procedure

To verify the HBM/MM waveform verification procedures, see ANSI/ESD STM5.1 and ANSI/ESD STM5.2 for further information.

6.3 Waveform Verification Following Servicing

Verify the waveforms meet all parameters specified after any repairs or servicing of the tester in compliance with ANSI/ESD STM5.1 and ANSI/ESD STM5.2.

7.0 ESD TESTING REQUIREMENTS AND PROCEDURES

7.1 Test Requirements

7.1.1 Handling of Components

Use ESD damage prevention procedures when handling components before, during and after testing.

7.1.2 Required Waveform Check

Verify waveform integrity described in Section 8.1.2 of ANSI/ESD STM5.1 and Section 7.4 of ANSI/ESD STM5.2.

7.1.3 High Voltage Discharge Path Check

Verify high voltage discharge path described in Section 8.1.3 of ANSI/ESD STM5.1 and Section 7.4 of ANSI/ESD STM5.2.

7.1.4 Component Static and Dynamic Tests

To determine whether components have failed, perform static and dynamic testing to all datasheet parameters before and after ESD testing. Pin leakage current may only be used as guides in determining the component ESD withstand voltage. It is not sufficient, especially for complex integrated circuits, to use pin leakage as the only criterion for component failure.

7.1.5 Pin Combinations

The pin combinations to be used for ESD stressing of all components are given in Table 1. Pin combination (n) is the total number of pin combinations. This varies from component to component depending on the number of power pin groups with the same name, Vps(i) in Table 1.

Table 1. Pin Combinations for HBM and MM Testing

Pin Combination Set	Connect Individually to Terminal A	Connect to Terminal B (Ground)	Floating Pins (Unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	Vps(1) [First power pin(s)]	All pins except pin under test (PUT) and Vps(1)[First power pin]
2	All pins one at a time, except the pin(s) connected to Terminal B	Vps(2) [Second power pin(s)]	All pins except PUT and Vps(2) [Second power pin]
i	All pins one at a time, except the pin(s) connected to Terminal B	Vps(i) [ith power pin(s)] [1,2, ...i]	All pins except PUT and Vps(i)
n-1	All pins one at a time, except the pin(s) connected to Terminal B	Vps(n-1)	All pins except PUT and Vps(n-1)
n	All non-Vps(i) pins one at a time.	All other non-Vps(i) pins, except the pin connected to Terminal A.	All Vps(i) pins

For those components with more pins than the ESD simulator tester channels, custom TFBs can be designed and constructed to reduce the total number of supply pins into groups of pins. The group supply pin, which could short together a small number of power and ground pins, would be connected to Terminal A or Terminal B per the requirements in Table 1. Annex A illustrates how this custom TFB can be built and how the group supply pins can be defined.

7.2 ESD Stress Testing Procedure

Perform ESD stress testing at room temperature in accordance with the procedure below. It is permissible to use any voltage level in Tables 2 or 3 as the starting stress level. Three new components may be used at each voltage level or pin combination if desired. This will eliminate any step stress hardening effects, and reduce the possibility of early failure due to cumulative stress on power pins (see NOTE 4 for more information). However, if a single set of three components is stressed at each level, then to avoid missing possible ESD vulnerability windows, it is recommended not to miss any stress step.

Table 2. HBM ESD Stress Levels

Stress Level	Equivalent Charging (±) Voltage Vp (volt)
1	250
2	500
3	1000
4	2000
5	4000
6	8000 (optional)

Table 3. MM ESD Stress Levels

Stress Level	Equivalent Charging (±) Voltage Vp (volt)
1	100
2	200
3	400

NOTE 2: A component may pass at 4000 volts but fail at 2000 volts. This is called a component fail window. To avoid this fail window, it is recommended that components be tested at each level defined in Table 2 (HBM) or Table 3 (MM).

Use the following procedure to ESD stress components:

7.2.1 Test a minimum of three samples of the component to all specified static and dynamic data sheet parameters.

7.2.2 Determine the starting stress voltage level from Table 2 (HBM) or Table 3 (MM). Select the first pin combination to be tested as stated in Section 7.1.5.

7.2.3 For HBM testing, apply one positive and one negative pulse to the component. Allow at least a 0.3 second interval between pulses. Repeat this process using all other pin combinations specified in Table 1.

7.2.4 For MM testing, apply three positive and three negative pulses to the component. Allow at least a 1.0 second interval between pulses. Repeat this process using all other pin combinations specified in Table 1.

NOTE 3: One pulse per polarity is used only for ANSI/ESD STM5.1 and is not permitted for ANSI/ESD STM5.2.

7.2.5 Test the components to full static and dynamic data sheet parameters and record the results for each component. Parametric and functional testing shall be performed at room temperature. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

If all three components pass the specified data sheet parameters, repeat steps 7.2.3 or 7.2.4, using the next higher stress level of Table 2 (HBM) or Table 3 (MM). Three new components may be used at each voltage level or pin combination if desired.

7.2.6 If one or more components fail, repeat the ESD stress test using three new components starting at the next lower stress level. If the components continue to fail, decrease the stress voltage until level 1 is reached in Table 2 (HBM) or Table 3 (MM). If any additional failures are observed at level 1, then stop all testing at this level.

8.0 FAILURE CRITERIA

A component is considered an ESD failure if it fails the data sheet parameters as specified in Section 7.1.4.

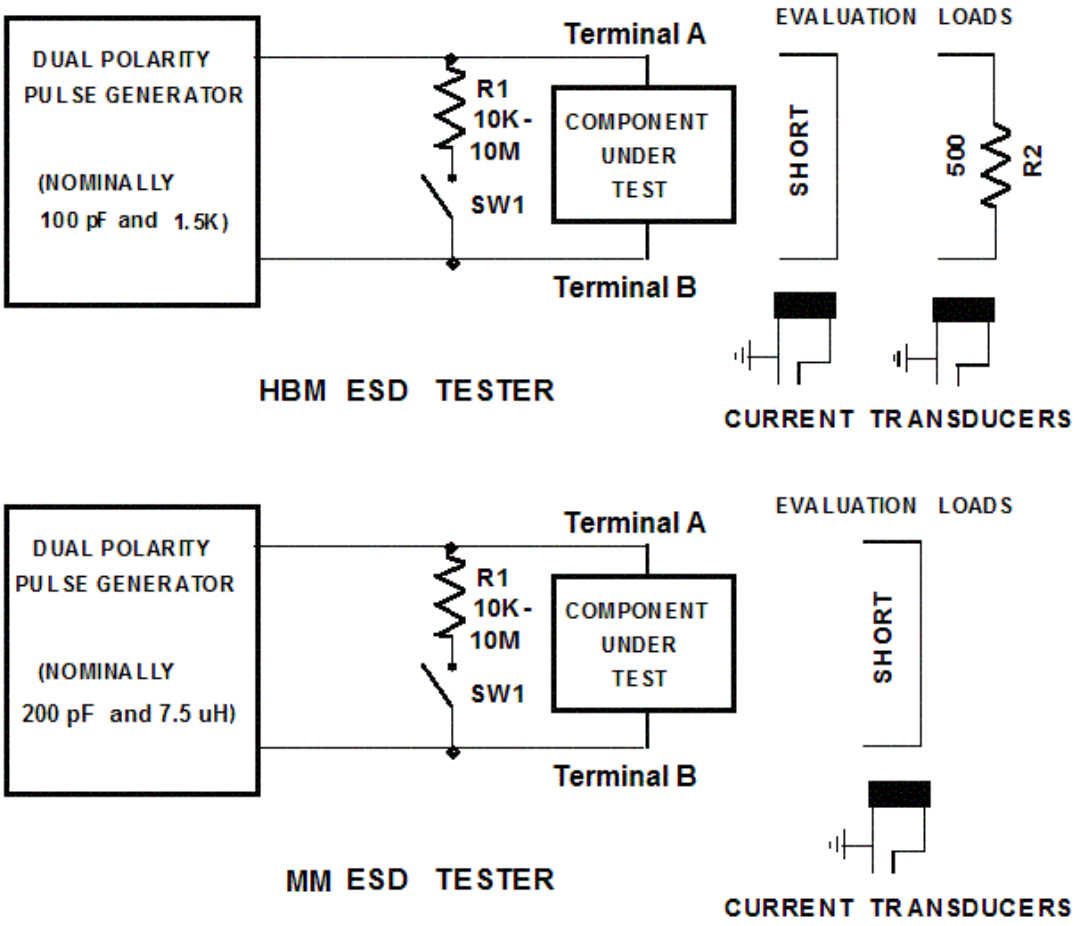


Figure 1. Typical Equivalent Stress Test Circuits

Requirements:

1. See ANSI/ESD STM5.1 for detailed HBM requirements.
2. See ANSI/ESD STM5.2 for detailed MM requirements.

(This annex is not part of ANSI/ESD SP5.1.1-2006)

ANNEX A – EXAMPLE OF POWER SUPPLY GANGING

In this example, the component has 756 pins and there are 512 channels on the tester. This means there are 244 more component pins than tester channel pins. Consequently, a custom test fixture board needs to be built that shorts together multiple Vdd and Vss pins together.

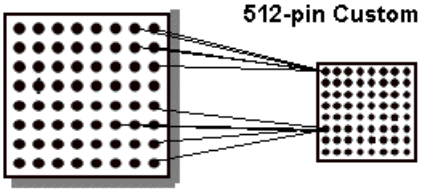
The component has 456 signal pins, 75 Vdd1, 75 Vdd2 and 150 Vss pins. All of the signal pins are individually wired to the custom test fixture board. The remaining 300 supply pins now must be assigned to the remaining 56 test channel pins.

The custom test fixture board can be built as follows:

1. 15 groups of Vdd1 gang pins (each group shorts together 5 Vdd1 pins).
2. 15 groups of Vdd2 gang pins (each group shorts together 5 Vdd2 pins).
3. 25 groups of Vss gang pins (each group shorts together 6 Vss pins).
4. 1 extra tester channel pin
5. Totals: 55 groups are allocated to 55 test channel pins.

The wiring of the custom test fixture board is illustrated in Figure 2.

Component A: 756 pins



(a) The power and ground pins are grouped together to reduce the effective pin count.

Component A	Pins
Signal Pins	456
Vdd1	75
Vdd2	75
Vss	150
Total	756

Custom TFB	Tester Channel Pins	# of Pins per Group	Component Pin Totals
Signal Pins	456	1	456 x 1 = 456
Vdd1	15	5	15 x 5 = 75
Vdd2	15	5	15 x 5 = 75
Vss	25	6	25 x 6 = 150
Spares	1	--	--
Total	512	--	756

(b) Vdd1 and Vdd2 have 15 groups of 5 pins wired together on the custom test fixture board, each group is connected to a Tester Channel pin.

Figure 2. Example of Supply Pin Ganging Method

For each group, one pin in the group will be wired on the custom test fixture board to connect to a single tester channel pin. These groups will make up a modified Vdd1, Vdd2 and Vss pin groups which would be used for Vps(1), Vps(2) and Vps(3) as shown in Table 1, Terminal B. When the Vdd1 group pin is placed in Terminal A and stressed, the entire group of 5 Vdd1 pins will be stressed as a single pin. This test step is different from ANSI/ESD STM5.1, so the HBM fail voltages may be slightly different from that method.

The construction of the custom test fixture board requires special wire configuration for the shorted power and ground pins. Figure 3 illustrates four different methods for wiring the pins together.

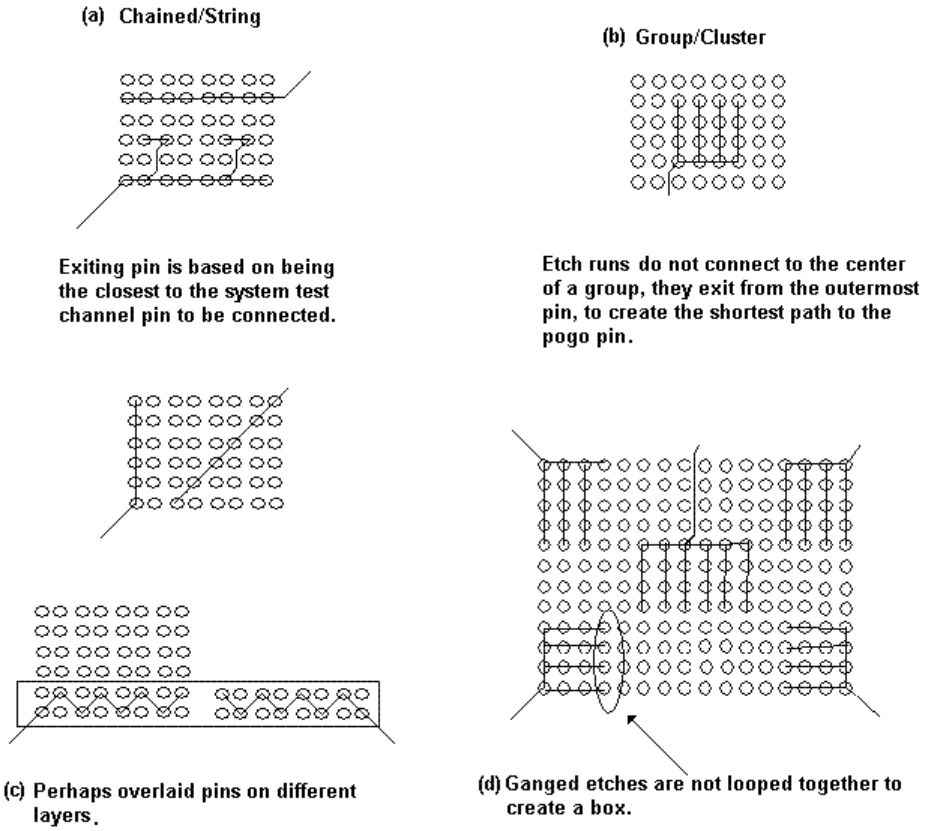


Figure 3. Printed Circuit Board (PCB) Layout Techniques for Ganging Supply Pins

NOTE 4: For those components (e.g., ball grid array) that interconnect different power leads through common, low-resistance power and ground planes in the package, the existing ANSI/ESD STM5.1 and ANSI/ESD STM5.2 test methods require that each individual power supply pin be stressed one at a time. Since all of the individual power supply leads are shorted in the package by the power or ground planes, repetitive stressing of each individual pin can result in cumulative ESD wear out failure mechanisms. This type of ESD test stress is to be avoided.

NOTE 5: Shorting the VCC pins or balls on the test fixture board introduces some extra inductance due to the wire trace connection shown in Figure 3. This extra inductance may result in slower discharge waveform rise times. At the same time, removing the extra VCC pins or balls from the tester reduces the tester background capacitance and may improve the discharge waveform. The net effect of applying this standard practice is to decrease unwanted interaction between the component and the tester.

(This annex is not part of ANSI/ESD SP5.1.1-2006)

ANNEX B – BIBLIOGRAPHY

MIL-STD-883D: Test Methods and Procedures for Microelectronics: Method 3015.7 Electrostatic Discharge Sensitivity Classification

MIL-STD-750C Notice 4: Test Methods for Semiconductor Devices: Method 1020: Electrostatic Discharge Sensitivity Classification