

ANSI/ESDA/JEDEC JS-001-2010

ESDA/JEDEC Joint Standard

ANSI/ANSI/ESDA/JEDEC JS-001-2010

Revision and Replacement of ANSI/ESD STM5.1-2007 &
JEDEC JESD22-A114F

*For Electrostatic Discharge
Sensitivity Testing*

*Human Body Model (HBM) -
Component Level*

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Approved April 20, 2010*

***ESDA/JEDEC Joint Standard for
Electrostatic Discharge Sensitivity Testing -***

***Human Body Model (HBM) -
Component Level***

Approved January 13, 2010
ESD Association & JEDEC Solid State Technology Association



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FOREWORD

This joint standard was developed under the guidance of the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices and the ESDA Standards Committee. The content was developed by a Joint Working Group composed of members of the JEDEC ESD Task Group and ESDA Working Group 5.1 (Human Body Model). The new standard is intended to replace the existing Human Body Model ESD standards (JESD22-A114F and ANSI/ESD STM5.1). It contains the essential elements of both standards. Data previously generated with testers meeting all waveform criteria of **either prior standard** shall be considered valid test data. HBM equipment which met either prior standard should also meet the joint standard requirements.

Some highlights of the changes that were made are included here. The scope and purpose of the two documents were merged. A clause declaring the acceptability of data obtained from both previous standards was included. Definitions from ESDA and JEDEC Glossary of Terms were used as appropriate and new definitions for failure window and for power pins connected to a package plane were added. Descriptions of oscilloscope and current transducers were refined and updated. The HBM circuit schematic and description was improved including references to pre-pulse and trailing pulse phenomena were made. Details for mitigating these effects were moved to an annex. The description of stress test equipment qualification and verification was completely re-written. Qualification and verification of test fixture boards was largely based on ANSI/ESD STM5.1. Two alternate daily verification procedures were defined. A new section on the determination of ringing in the current waveform was added. The basic pin combinations and stressing were the same in both documents. Some alternate pin combinations, which had been adopted in JESD22-A114F and were under consideration in ANSI/ESD STM5.1 at the time this merged version was initiated, were included. Failure and classification criteria were the same in both documents and were not changed in this document.

In the future this standard will be maintained and revised as a Joint Standard through a Memorandum of Understanding between JEDEC and ESDA. The merger of the two HBM ESD standards will now eliminate any confusion or misunderstandings that previously may have occurred in the industry. This standard is a living document and revisions and updates will be made on a routine basis driven by the needs of the electronic industry.

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ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level

1.0 SCOPE AND PURPOSE

1.1 Scope

This standard establishes the procedure for testing, evaluating, and classifying components and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

1.2 Purpose

The purpose (objective) of this standard is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

1.2.1 Existing Data

Data previously generated with testers meeting all waveform criteria of **ANSI/ESD STM5.1-2007** or **JESD22 – A114F** shall be considered valid test data.

2.0 REFERENCES

ESD ADV1.0, ESD Association's Glossary of Terms¹

JESD99B JEDEC Standard, May 2007 - Terms, Definitions, and Letter Symbols for Microelectronic Devices²

ANSI/ESD STM5.1-2007, ESD Association Standard Test Method for Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) Component Level¹

JESD22 – A114F, December 2008, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)²

3.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms and JESD99B JEDEC Standard, May 2007 – Terms, Definitions, and Letter Symbols for Microelectronic Devices.

Component. An item such as a resistor, diode, transistor, integrated circuit or hybrid circuit. A component may also be referred to as a device.

Component failure. A condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters.

Data sheet parameters. The static and dynamic component performance data supplied by the component manufacturer or supplier.

Dynamic parameters. Parameters measured with the component in an operating condition. These may include, but are not limited to full functionality, output rise and fall times under a specified load condition, and dynamic current consumption.

ESD withstand voltage. The highest voltage level that does not cause device failure; the device passes all tested lower voltages (see Failure Window).

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Failure Window. An intermediate range of stress voltages that can induce failure in a particular device type, when the device type can pass some stress voltages both higher and lower than this range. For example, a component with a failure window may pass a 500 volt test, fail a 1000 volt test and pass 2000 volt test. The withstand voltage of this device is 500 volts.

HBM ESD tester. Equipment (also referred to as "tester" in this standard) that applies an HBM ESD to a component. Also referred to as an HBM Simulator.

Human Body Model (HBM) ESD. An ESD event meeting the waveform criteria specified in this standard, approximating the discharge from the fingertip of a typical human being.

Ips. The peak current value is determined by the current at time t_{max} on the linear extrapolation of the exponential current decay curve. The linear extrapolation should be based on the current waveform data over a 40 nanosecond period beginning at t_{max} . (See Figure 2A)

Ips_{max}. The peak current maximum value is the highest current value measured. This value includes the overshoot or ringing components due to internal test simulator RLC parasitics. (See Figure 2A)

No Connect Pin. A package interconnect (pin, bump or ball) that is not electrically connected to a die.

Package Plane. A low impedance metal layer built into an IC package connecting a group of bumps or pins (typically power or ground). There may be multiple package planes (sometimes referred to as islands) for each power and ground group.

Pre-Pulse Voltage. A voltage occurring at the device under test (DUT) just prior to the generation of the HBM current pulse. (See Annex C.2)

Pulse Generation Circuit. The circuit network that produces a human body discharge current waveform. Also referred to as Dual Polarity Pulse Source.

Ringing. A high frequency oscillation superimposed on a waveform.

Shorted non-supply pin. Any non-supply pin (typically an I/O pin) that is metallurgically connected (typically < 3 ohm) on the chip or within the package to another non-supply pin (or set of non-supply pins).

Spurious current pulses. Small HBM shaped pulses that follow the main current pulse, and are typically defined as a percentage of Ips_{max} .

Static parameters. Parameters measured with the component in a non-operating condition. These may include, but are not limited to, input leakage current, input breakdown voltage, output high and low voltages, output drive current, and supply current.

Step stress test hardening. This occurs when a component subjected to increasing ESD voltage stresses is able to withstand higher stress levels than a similar component not previously stressed. For example: a component may fail at 1000 volts if subjected to a single stress, but fail at 3000 volts if stressed incrementally from 250 volts.

Test Fixture Board. A test fixture board is a specialized circuit board, with one or more component sockets, which connects the DUT(s) to the HBM simulator.

t_{max} . The time when Ips is at its maximum value (Ips_{max}). (See Figure 2A)

Trailing current pulse. A current pulse that occurs after the HBM current pulse has decayed. (See Annex C.1) A trailing current pulse is a relatively constant current often lasting for hundreds of microseconds.

4.0 APPARATUS AND REQUIRED EQUIPMENT

4.1 Waveform Verification Equipment

All equipment used to evaluate the tester shall be calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current transducer and high voltage resistor load. Maximum time between calibrations shall be one year. Calibration shall be traceable to national standards, such as the National Institute of Standards and Technology (NIST) in the United States, or comparable international standards.

Equipment capable of verifying the pulse waveforms defined in this standard test method includes, but is not limited to, an oscilloscope, evaluation loads and a current transducer.

4.1.1 Oscilloscope

A digital oscilloscope is recommended but analog oscilloscopes are also permitted. In order to insure accurate current waveform capture, the oscilloscope shall meet the following requirements:

- a. Minimum sensitivity of 100 milliamperes per major division when used in conjunction with the current transducer specified in Section 4.1.2.
- b. Minimum bandwidth of 350 MHz.
- c. For analog scopes, minimum writing rate of one major division per nanosecond.

4.1.1.1 Additional Requirements for Digital Oscilloscopes

- a. Recommended channels: 2 or more
- b. Minimum sampling rate: 1 GS/s
- c. Minimum vertical resolution: 8-bit
- d. Minimum vertical accuracy: $\pm 2.5\%$
- e. Minimum time base accuracy: 0.01%
- f. Minimum record length: 10 k points

4.1.2 Current Transducer (Inductive Current Probe)

- a. Minimum bandwidth of 200 MHz.
- b. Peak pulse capability of 12 amperes.
- c. Rise time of less than 1 nanosecond.
- d. Capable of accepting a solid conductor as specified in Section 4.1.3.
- e. Provides an output voltage per signal current as required in Section 4.1.1.
(This is usually between 1 and 5 millivolts per milliamperes.)

4.1.3 Evaluation Loads

Two evaluation loads are necessary to verify tester functionality:

- a. Load 1: A solid 18–24 AWG (standard non-US wire size 0.75 to 0.25 mm² cross-section) tinned copper shorting wire as short as practicable to span the distance between the two farthest pins in the socket while passing through the current probe.
- b. Load 2: A 500 ohm, $\pm 1\%$, minimum 4000 voltage rating, low-inductance resistor shall be used for initial system checkout and periodic system recalibration.

4.2 Human Body Model Simulator

A simplified schematic of the HBM simulator or tester is given in Figure 1. The performance of the tester is influenced by parasitic capacitance and inductance. Thus, construction of a tester using this schematic does not guarantee that it will provide the HBM pulse required for this standard. The waveform capture procedures and requirements described in Section 5 determine the acceptability of the equipment for use.

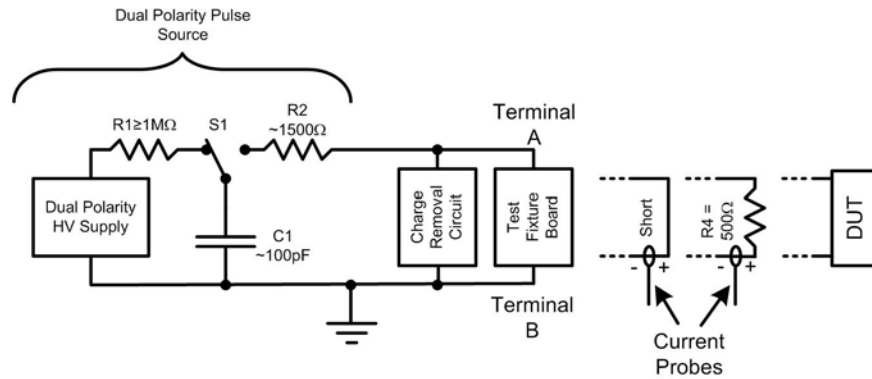


Figure 1: Simplified HBM Simulator Circuit with Loads

NOTES:

1. The current transducers (probes) are specified in Section 4.1.2.
2. The shorting wire (Short) and 500 ohm resistor (R4) are evaluation loads specified in Section 4.1.3.
3. Reversal of Terminals A and B to achieve dual polarity performance is not permitted.
4. The charge removal circuit ensures a slow discharge of the device, thus avoiding the possibility of a charged device model discharge. A simple example is a 10 kohm or larger resistor (possibly in series with a switch) in parallel with the test fixture board. This resistor may also be useful to control parasitic pre-pulse voltages (See Annex C).
5. The Dual Polarity Pulse Generator (Source) shall be designed to avoid recharge transients and double pulses.
6. Stacking of DUT socket adapters (piggybacking or the insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of this standard defined in Table 1.
7. Component values are nominal.

4.2.1 HBM Test Equipment Parasitic Properties

Some HBM simulators have been found to falsely classify HBM sensitivity levels due to parasitic artifacts or uncontrolled voltages unintentionally built into the HBM simulators. Methods for determining if these effects are present and optional mitigation techniques are described in Annex C.

5.0 STRESS TEST EQUIPMENT QUALIFICATION AND ROUTINE VERIFICATION

5.1 Overview of Required HBM Tester Evaluations

The HBM tester and test fixture boards shall be qualified, re-qualified, and periodically verified as described in this section. **The safety precautions described Section 5.8 should be followed at all times.**

5.2 Measurement Procedures

5.2.1 Reference Pin Pair Determination

The two pins of each socket on a test fixture board which make up the reference pin pair are (1) the socket pin with the shortest wiring path to the pulse generation circuit (Terminal B) and (2) the socket pin with the longest wiring path from the pulse generation circuit (Terminal A) to the ESD stress socket. (See Figure 1). This information is typically provided by the equipment or test fixture board manufacturer. If more than one pulse generation circuit is connected to a socket then there may be more than one reference pin pair.

It is recommended that on non-positive clamp fixtures, feed through test point pads be added on these paths. These test points should be added as close as possible to the socket(s).

NOTE: A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. It allows the shorting wire to be easily clamped into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

5.2.2 Waveform Capture with Current Probe

To capture a current waveform between two socket pins (usually the reference pin pair), use the shorting wire (Section 4.1.3, Load 1) for the short circuit measurement or the 500 ohm resistor (Section 4.1.3, Load 2) for the 500 ohm current measurement and the inductive current probe (Section 4.1.2).

5.2.2.1 Short Circuit Current Waveform

Attach the shorting wire between the pins to be measured. Place the current probe around the shorting wire, as close to Terminal B as practical, observing the polarity shown in Figure 1. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification or periodic verification being conducted.

- a. For positive clamp sockets, insert the shorting wire between the socket pins connected to Terminals A and B and hold in place by closing the clamp.
- b. For non-positive clamp sockets, attach the shorting wire between the socket pins connected to Terminals A and B. If it is not possible to make contact within the socket, connect the shorting wire between the reference pin pair test points or socket mounting holes, if available.

5.2.2.2 500 ohm Load Current Waveform

Attach the 500 ohm resistor between the pins to be measured. The current probe shall be placed around the wire between the resistor and Terminal B. Apply an ESD stress at the voltage and polarity needed to execute the qualification, re-qualification or periodic verification being conducted. Follow procedure according to socket type as described in Section 5.2.2.1.

5.2.3 Determination of Waveform Parameters

The captured waveforms are used to determine the parameter values listed in Table 1.

5.2.3.1 Short Circuit Waveform

Typical short circuit waveforms are shown in Figures 2A and 2B. The parameters I_{ps} (peak current), t_r (pulse rise time), t_d (pulse decay time) and I_R (ringing) are determined from this waveform. Ringing may prevent the simple determination of I_{ps} . A graphical technique for determining I_{ps} and I_R is described in Section 5.2.3.3 and Figure 4.

5.2.3.2 500 Ohm Load Waveform

A typical 500 ohm load waveform is shown in Figure 3. The parameters I_{pr} (peak current with 500 ohm load) and t_{rr} (pulse rise time with 500 ohm load) are determined from this waveform.

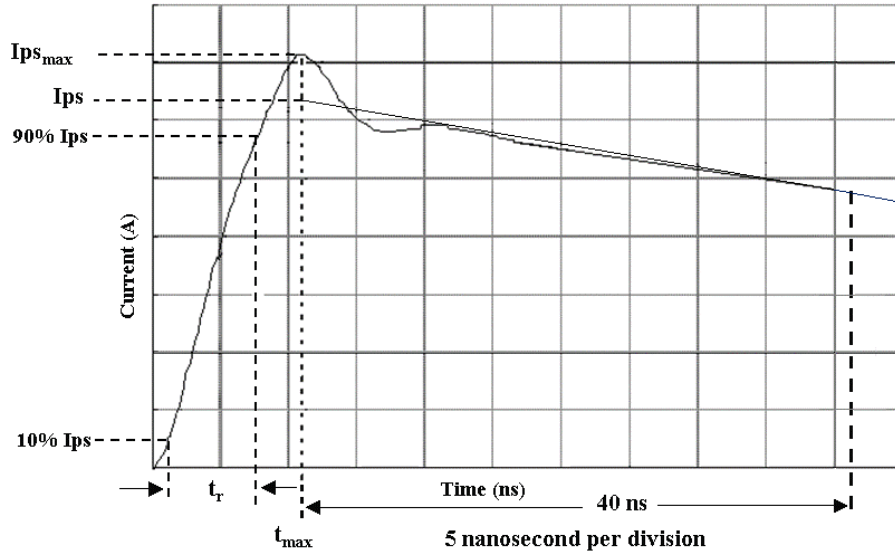


Figure 2A: Current Waveform through a Shorting Wire ($I_{ps_{max}}$)

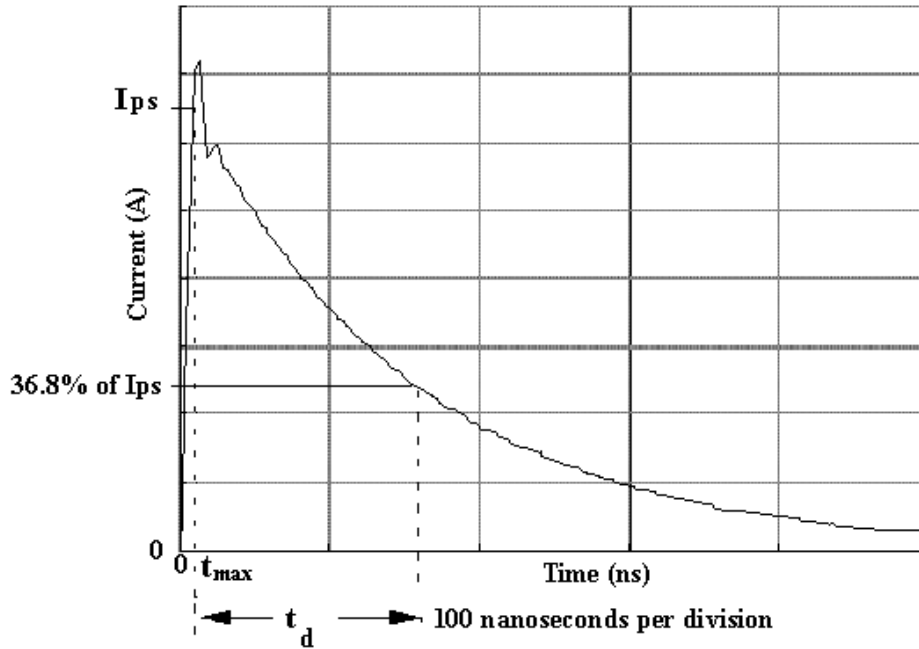


Figure 2B: Current Waveform through a Shorting Wire (t_d)

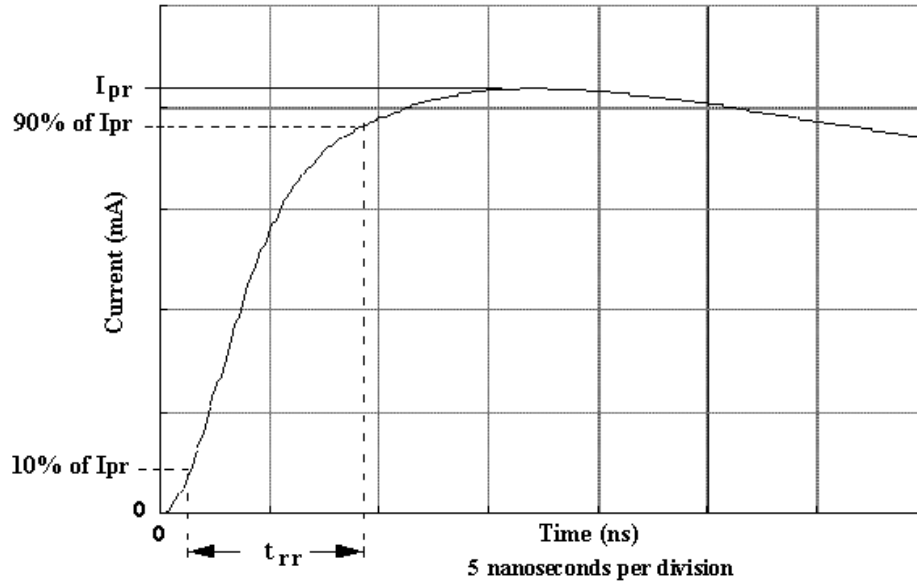


Figure 3: Current Waveform through a 500 ohm Resistor

5.2.3.3 Graphical Determination of I_{ps} and I_R (See Figure 4)

5.2.3.3.1 A line is drawn (manually or using numerical methods such as least squares) through the HBM ringing waveform from t_{max} to $t_{max} + 40$ ns to interpolate the value of the curve for a more accurate derivation of the peak current value (I_{ps}). t_{max} is the time when $I_{ps_{max}}$ occurs (see definition for t_{max} in Section 3 and Figure 2A).

5.2.3.3.2 The maximum deviation of the measured current above the straight line fit is Ring1. The maximum deviation of the measured current below the straight line fit is Ring2. The percent ringing is defined as:

$$\% \text{ Ring} = (|Ring1| + |Ring2|) / I_{ps} \times 100$$

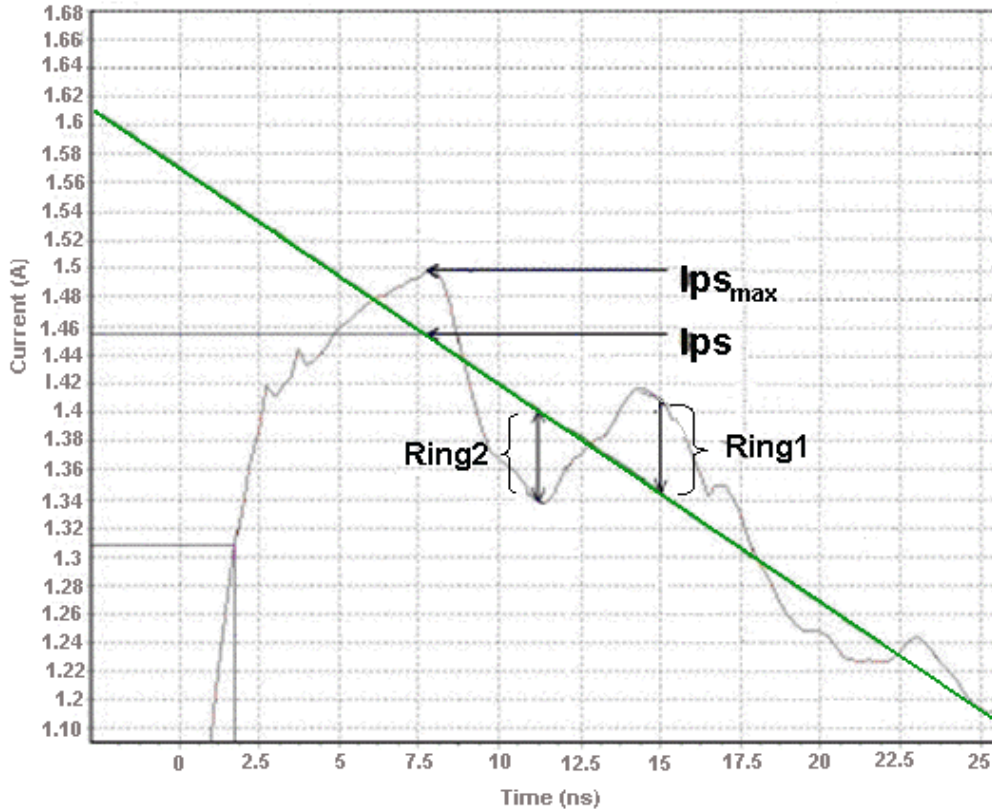


Figure 4: Peak Current Short Circuit Ringing Waveform

5.2.4 High Voltage Discharge Path Test

This test is intended to ensure that the tester high voltage relays and the grounding relays that connect pulse generator(s) and grounds to the DUT are functioning properly. The tester manufacturer should provide a recommended procedure and if needed, a verification board and software.

5.3 HBM Tester Qualification

HBM ESD tester qualification as described in this section is required in the following situations:

- Acceptance testing when the ESD tester is delivered or first used.
- Periodic re-qualification in accordance with manufacturer's recommendations. The maximum time between re-qualification tests is one year.
- After service or repair that could affect the waveform.

5.3.1 HBM Tester Qualification Procedure

5.3.1.1 Test Fixture Board, Socket and Pins

Use the highest pin count test fixture board with a positive clamp socket for the tester waveform verification or the recommended Waveform Verification Board provided by the manufacturer.

The reference pin pair(s) of the highest pin count socket on the board shall be used for waveform capture. Waveforms from every pulse generating circuit are to be recorded.

Electrical continuity for all pins on the test fixture board shall be verified prior to qualification testing. This can typically be done using the manufacturer's recommended self-test.

5.3.1.2 Short Circuit Waveform Capture

- a. Configure the test fixture board, shorting wire, and transducer for the short circuit waveform measurement as described in Section 5.2.2.1.
- b. Apply five positive and five negative pulses at each test voltage. Record waveforms at 1000, 2000 and 4000 volts. Verify that the waveforms meet all parameters specified in Figures 2A and 2B and Table 1.

5.3.1.3 500 ohm Load Waveform Capture

- a. Configure the test fixture board, resistor, and transducer for the 500 ohm load waveform measurement as described in Section 5.2.2.2.
- b. Record waveforms at 1000 and 4000 volts, both positive and negative polarities. Verify that the waveforms meet all parameters specified in Figure 3 and Table 1.

5.3.1.4 Spurious Current Pulse Detection

Secondary pulses after the HBM pulses are generated by the discharge relay. Using the shorting wire configuration, initiate a 1000 volt pulse and verify that any pulses after the initial HBM pulse are less than 15% of the amplitude of the main pulse.

NOTE: For analog oscilloscopes, setting the time base to 1 millisecond/division can detect these types of pulses. For digital oscilloscopes, current pulses after the initial current pulse can be observed, but advanced triggering functions such as sequential triggering or delayed triggering may be needed so secondary pulses are not missed due to low sampling rates.

5.4 Test Fixture Board Qualification

Test fixture boards shall be qualified in a qualified tester prior to initial use or after repair. This procedure is also required when a previously qualified test fixture board is used in a different model HBM simulator from the one in which it was originally qualified. The procedure shall be applied to the reference pin pairs on all sockets of the new test fixture board. If there is not adequate physical access to the socket, follow the guidance of Section 5.2.2.1b.

5.4.1 Configure the test fixture board, shorting wire, and current probe for the short circuit waveform measurement as described in Section 5.2.2.1 with a qualified tester.

5.4.2 Apply at least one positive and one negative 1000 volt pulse. All waveform parameters shall be within the limits specified in Figures 2A and 2B and Table 1.

5.4.3 Configure the test fixture board, 500 ohm resistor, and transducer for the 500 ohm load waveform measurement as described in Section 5.2.2.2.

5.4.4 Apply at least one positive and one negative 1000 volt pulse. All waveform parameters shall be within the limits specified in Figure 3 and Table 1.

5.4.5 Repeat for all additional reference pin pairs of all pulse generating circuits and sockets.

Table 1. Waveform Specification

Voltage Level (V)	I _{peak} for Short, I _{ps} (A)	I _{peak} for 500 Ω I _{pr} (A)	Rise Time for Short, t _r (ns)	Rise Time for 500 Ω t _{rr} (ns)	Decay Time for Short, t _d (ns)	Maximum Ringing Current I _R (A)
250	0.15-0.19	N/A	2.0-10	N/A	130-170	15% of I _{ps}
500	0.30-0.37	N/A	2.0-10	N/A	130-170	15% of I _{ps}
1000	0.60-0.74	0.37-0.55	2.0-10	5.0-25	130-170	15% of I _{ps}
2000	1.20-1.48	N/A	2.0-10	N/A	130-170	15% of I _{ps}
4000	2.40-2.96	1.5-2.2	2.0-10	5.0-25	130-170	15% of I _{ps}
8000 (optional)	4.80-5.86	N/A	2.0-10	N/A	130-170	15% of I _{ps}

5.5 Routine Waveform Check Requirements

5.5.1 Standard Routine Waveform Check Description

Waveforms shall be acquired using the short circuit method (Section 5.2.2.1) on the reference pin pair for each socket. If necessary, the test fixture board being used may be removed and replaced with a positive clamp socket test fixture board to facilitate waveform measurements. Stresses shall be applied at positive and negative 1000 volts or the stress level to be tested during the use. The waveforms shall meet the requirements of Figures 2A and 2B and Table 1.

5.5.1.1 Waveform Check Frequency.

The waveforms shall be verified according to this procedure at least once per shift. If ESD stress testing is performed in consecutive shifts, waveform checks at the end of one shift may also serve as the initial check for the following shift.

Longer periods between waveform checks may be used if no changes in waveforms are observed for several consecutive checks. Simpler waveform checks (Section 5.5.2) may be used with longer period between waveform checks as described in this section. For example, Section 5.5.2 tests may be done daily with tests according to Section 5.5.1 done monthly. The test frequency and method chosen shall be documented. If at any time the waveforms no longer meet the specified limits, all ESD stress test data collected subsequent to the previous satisfactory waveform check shall be marked invalid and shall not be used for classification.

If the tester has multiple pulse generation circuits, then the waveform for each pulse generation circuit shall be verified with a positive clamp socket test fixture board. The recommended time period between verification tests is once per shift. However, a rotational method of verification

may be used to ensure all pulse generation circuits are functioning properly. For instance, on day 1, pulse generation circuit 1 would be tested. On day 2, pulse generation circuit 2 would be tested and on day 3, pulse generation circuit 3 would be tested, until all circuits have been tested, at which time circuit 1 would again be tested. The recommended maximum interval between tests of any one pulse generator is two weeks. However, if a pulse generation circuit fails, then all ESD stress tests subsequent to the previous satisfactory waveform check of that pulse generation circuit shall be marked invalid and shall not be used for classification.

5.5.2 ALTERNATE ROUTINE WAVEFORM CAPTURE PROCEDURE

As an alternative to the detailed routine waveform analysis, a quick pass/fail waveform capture process can be instituted for routine verification. This method may be used in combination with Section 5.5.1 as described above.

5.5.2.1 Capture a waveform using a shorting wire evaluation load at +1000 volts.

5.5.2.2 Measure $I_{ps_{max}}$ (without adjustment for ringing) and ensure that it is between 0.60 and 0.74 ampere.

5.5.2.3 Repeat at -1000 volts.

5.5.2.4 If the tester has multiple pulse sources, choose a pin pair combination from a different pulse source each day, rotating through each pulse source in turn as described in Section 5.5.1.1.

If $I_{ps_{max}}$ is within the values specified for both polarities and the waveforms appear normal, the tester is considered ready to use.

NOTE: This measurement doesn't take into consideration I_{ps} ringing; this may affect the results. If there are any concerns about how the waveforms look, or if the measurements are close to the upper or lower specification limits, a complete waveform analysis (Section 5.3.1) shall be performed.

NOTE: The quick pass/fail test method should be applied only to qualified test fixture boards for qualified ESD simulators. Test fixture boards and ESD simulator shall be qualified together using the test method in Section 5.3.1 before using test method Section 5.5.2.

5.6 High Voltage Discharge Path Check

This test is required for either routine check method (Section 5.5). Test the high voltage discharge and grounding paths and all associated circuitry at the beginning of each day during which ESD stress testing is performed. The period between self-test diagnostic checks may be extended, providing test data supports the increased interval. Use the tester manufacturer's recommended procedure. If any failure is detected, do not perform device testing with the sockets that are connected to the defective discharge paths. Repair the tester and then verify that the failed pins pass the self-test before resuming testing. Depending on the extent of the repair it may be necessary to perform a complete re-qualification according to Section 5.3.1.

5.7 Tester Waveform Records

5.7.1 Tester and Test Fixture Board Qualification Records

Retain the waveform records until the next re-qualification or for the duration specified by the user's internal record keeping procedures.

5.7.2 Periodic Waveform Check Records

Retain the periodic waveform records at least one year for the duration specified by the user's internal record keeping procedures.

5.8 Safety

5.8.1 Initial Set-up

During initial equipment set-up, a safety engineer or applicable safety representative shall inspect the equipment in its operating location to ensure that the equipment is not operated in a combustible (hazardous) environment.

5.8.2 Training

All personnel shall receive system operational training and electrical safety training prior to using the equipment.

5.8.3 Personnel Safety

The procedures and equipment described in this document may expose personnel to hazardous electrical conditions. Users of this document are responsible for selecting equipment that complies with applicable laws, regulatory codes and both external and internal policy. Users are cautioned that this document cannot replace or supersede any requirements for personnel safety.

Ground fault circuit interrupters (GFCI) and other safety protection should be considered wherever personnel might come into contact with electrical sources.

Electrical hazard reduction practices should be exercised and proper grounding instructions for equipment shall be followed.

6.0 CLASSIFICATION PROCEDURE

The devices used for classification testing must have completed all normal manufacturing operations. Testing must be performed using an actual device chip. It is not permissible to use a test chip representative of the actual chip or to assign threshold voltages based on data compiled from a design library or via software simulations. ESD classification testing shall be considered destructive to the component, even if no component failure is detected.

NOTE: Test chip in this case means ESD test structure.

6.1 Parametric and Functional Testing

Prior to ESD stressing, parametric and functional testing using conditions required by the applicable part drawing or test specification shall be performed on all devices submitted. Parametric and functional test results shall be within the limits stated in the part drawing for these parameters.

6.2 Devices For Each Voltage Level

A sample of three devices for each voltage level shall be characterized for the device ESD failure threshold using the voltage levels shown in Table 1. Finer voltage steps may optionally be used to obtain a more accurate measure of the failure threshold, and to improve detection of devices exhibiting failure windows. ESD testing should begin at the lowest level in Table 1 but may begin at any level. However, if the initial voltage level is higher than the lowest level in Table 1, and the device fails at the initial voltage, testing shall be restarted with three fresh devices at the next lowest level. (e.g. If the initial voltage is 1000 volts and the device fails, restart the test at 500 volts.) The ESD test shall be performed at room temperature.

Three new components may be used at each voltage level or pin combination if desired. This will eliminate any step-stress hardening effects, and reduce the possibility of early failure due to cumulative stress. Due to potential failure windows, low ESD performance may not be detected if levels specified in Table 1 are skipped during testing. It is recommended not to skip any levels specified in Table 1.

For each voltage level a sample of 3 devices shall be stressed using 1 positive and 1 negative pulse with a minimum of 100 milliseconds between pulses per pin for all pin combinations specified in Table 2.

NOTE: In some ESD simulators, a charge removal circuit is not present. For these simulators, increasing the time between pulses to prevent a charge build-up is one method to reduce the risk for subsequent pin overstress. Alternatively, curve trace leakage tests after each pulse for all pins in the DUT will also remove this excess charge stored in the test fixture board or socket.

It is permitted to use a separate sample of three devices for each pin combination set specified in Table 2. It is permitted to further partition each pin combination set in Table 2 and use a separate sample of three devices for each subset within the pin combination set. Separate samples may be used for different polarities.

6.3 Pin Categorization

Classification testing is performed using the pin combinations as defined in Table 2. Therefore, each pin must be categorized as a supply pin, a non-supply pin, or a no connect (NC). One or more supply pins can form a supply pin group as explained in Section 6.3.2.

6.3.1 Supply Pins

A supply pin is any pin that provides current to the circuit. While most supply pins are labeled such that they can be easily recognized as supply pins (examples: VDD, VDD1, VDD2, VDD_PLL, VCC, VCC1, VCC2, VCC_ANALOG, GND, AGND, DGND, VSS, VSS1, VSS2, VSS_PLL, VSS_ANALOG, etc.), others are not and require engineering judgment based on their function in the normal circuit operation (examples: Vbias, Vref, etc.). Supply pins typically transmit no information such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

An example of a pin that appears to be a supply pin but may be treated as a non-supply pin is the VPP pin on EPROM memories. The VPP puts the memory into a special, rarely used, programming state and supplies the high voltage needed for programming the memory.

6.3.2 Supply Pin Groups

The supply pins are partitioned into Supply Pin Groups with each supply pin a member of one and only one Supply Pin Group. Supply pins that are not connected by metal to any other pins are single pin Supply Pin Groups. Supply pins that are interconnected by metal on the chip or within the package form a supply pin group. The metal interconnects should be verified through reliable device documentation. However, excessive metal trace resistance in the die interconnect associated with grouping these pins could lead to masking an ESD protection weakness in HBM testing.

NOTE: If the pin inter-connect design is unknown, either measure the resistance between supply pins to determine the supply pin groups or treat each pin as a separate group.

NOTE: If the resistance between any two pins is greater than 3 ohms, the pins should be placed into separate Supply Pin Groups.

Table 2 is organized by the DUT's N supply pin groups. The first N rows of Table 2 have one unique supply pin group tied to ground. When pins are not connected by a package plane, pins within a supply pin group shall be stressed individually (when connected to Terminal A). When tied to ground (Terminal B), as shown in Table 2, these pins shall all be grounded either individually or tied together at the test board level.

6.3.2.1 Supply Pins Connected by Package Plane.

If a set of supply pins are connected by a package plane, as few as one pin (selected arbitrarily) from that set of pins may be used to represent the entire set as a supply pin group. The remaining pins in the set need not be stressed nor grounded and may be left floating during all testing.

NOTE: For example, if a supply pin group of 25 pins consists of five pins connected by metal only at the die level and 12 additional pins connected with one package plane and another with eight pins connected with a second package plane, the group may be represented by the five die-level connected pins and at least one pin from each package plane connected sets.

6.3.3 Other Supply Pin Types

Any pin that is intended to be pumped above the positive supply or below the negative supply of its circuit block shall be treated as a supply pin (example: positive and negative terminal pins connected to a charge pump capacitor).

Any pin that is connected to an internal power bus (or a power pin) by metal as described in Section 6.3.2 shall be treated as a supply pin (example: a Vdd sensing pin).

Any pin that is intended to supply power to another circuit on the same chip must be treated as a supply pin. However, if a pin is intended to supply power to a circuit on another chip but not to any circuit on the same chip, it may be treated as a non-supply pin.

6.4 No-Connect Pins

Pins labeled as no-connect pins but found to have an electrical connection to the die shall be tested as non-supply pins. Verified no-connect pins must not be stressed and must be left floating at all times.

6.5 Non-Supply Pins

All pins not categorized as supply pins or no connects are Non-Supply Pins. This includes pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins and VPP pins on EPROM memory. Most non-supply pins transmit information such as digital or analog signals, timing, clock signals, and voltage or current reference levels.

6.5.1 Non-Supply to Non-Supply Combinations

Pin combination set N+1 in Table 2 specifies to stress each non-supply pin individually (Terminal A) with all other remaining non-supply pins tied together and connected to Terminal B (except for those shorted non-supply pins that are metal connected to the pin under stress on the die, which will be left open).

If a device has non-supply pins that are connected on the die and bonded out to multiple separate pins, then these pins shall be stressed individually according to combination set N+1 with the remainder of these connected pins left floating.

6.5.2 Alternative Non-Supply to Non-Supply Combinations

It is permitted to partition the non-supply pins to be connected to Terminal B into two or more subsets, such that each of these pins is a member of at least one subset. The pin connected to Terminal A is to be stressed to each of these subsets separately. This process is repeated for each non-supply pin.

Table 2. Pin Combination Sets for Integrated Circuits

Pin Combination Set	Connect Individually to Terminal A	Connect to Terminal B (Ground)	Floating Pins (unconnected) (Must include no-connect pins)
1	All pins one at a time, except the pin(s) connected to Terminal B	First supply pin group	<i>All pins except PUT* and first supply pin group</i>
2	All pins one at a time, except the pin(s) connected to Terminal B	Second supply pin group	<i>All pins except PUT and second supply pin group</i>
N	All pins one at a time, except the pin(s) connected to Terminal B	Nth supply pin group	<i>All pins except PUT and Nth supply pin group</i>
N+1	Each Non-supply pin one at a time	All other Non-supply pins collectively except PUT	<i>All supply pins (See Section 6.6)</i>

* PUT = Pin under test.

6.6 Alternative Pin Stress Method for Non-Supply Pins

A non-supply to supply pin stress in Table 2 may be replaced by its corresponding supply pin to non-supply pin stress. If only a single polarity stress is being replaced, the opposite polarity stress shall be used. As non-supply pins are not typically tied to other pins, this will require each supply pin of the supply pin group to be stressed to each non-supply pin individually. If the non-supply pin is tied to other pins, they shall be left floating.

Typically, the non-supply to supply pin negative polarity stress will be replaced with the supply to non-supply pin, positive polarity stress. This allowance is useful when the slew rate of the HBM pulse is impacted by parasitic capacitance of the open relays.

NOTE: If this alternative test method is used on a supply pin group that has more than a small number of pins, tester parasitic capacitance will increase (i.e., slow down) the rise time of the signal. Longer rise times may cause dynamic ESD protection circuits not to function properly (See Annex C.3).

6.7 Testing After Stressing

If a different sample group is tested at each stress level, it is permitted to perform the DC parametric and functional testing after all sample groups have been ESD tested.

7.0 FAILURE CRITERIA

A part is defined as a failure if it fails the datasheet parameters using parametric and functional testing. If testing is required at multiple temperatures, testing shall be performed at the lowest temperature first.

8.0 COMPONENT CLASSIFICATION

ESD sensitive components are classified according to their HBM withstand voltage, regardless of polarity, as defined in Table 3.

Table 3. HBM ESD Component Classification Levels

Classification	Voltage Range (V)
0	< 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

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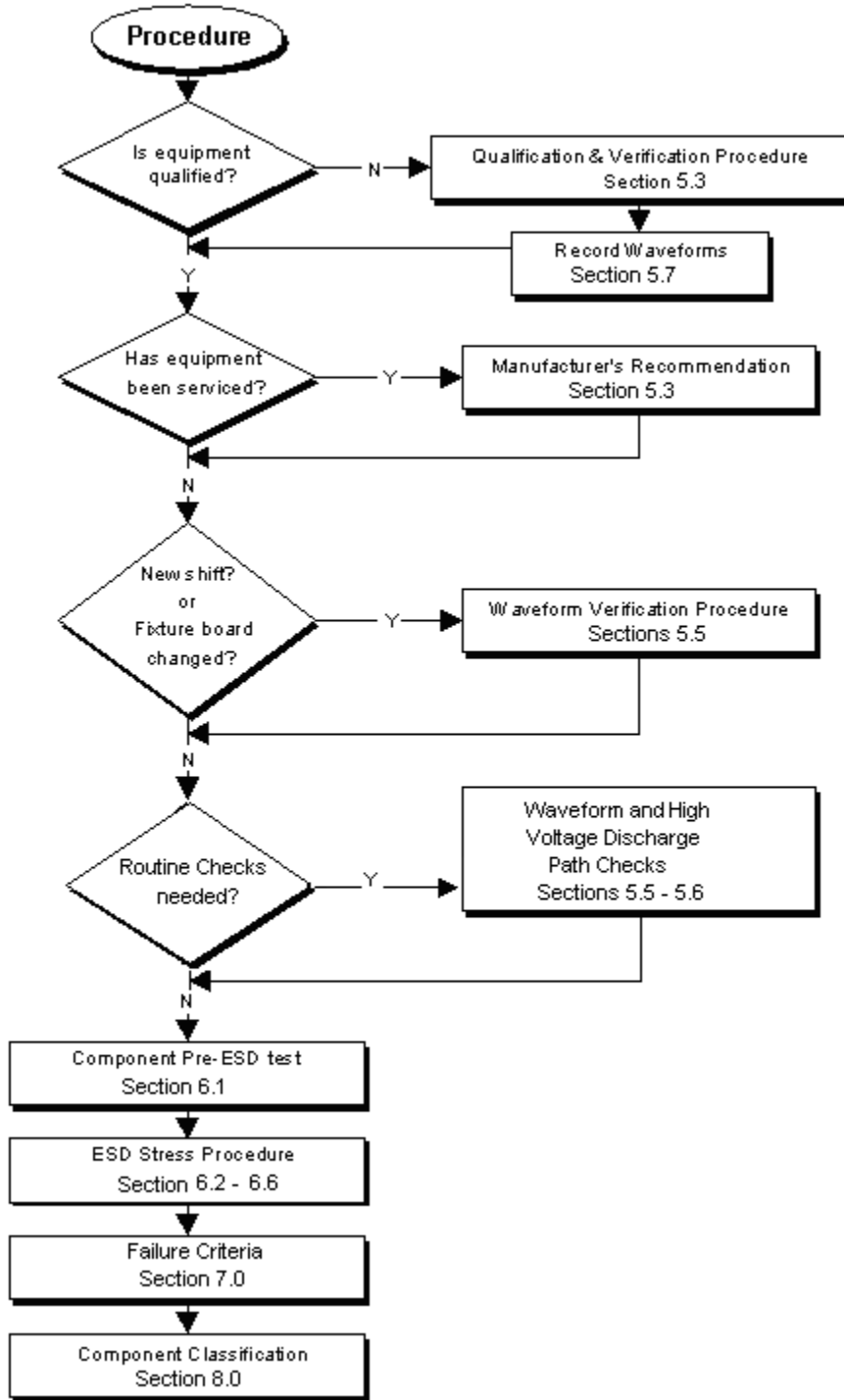
ANNEX A - INFORMATIVE – EXAMPLE OF PIN COMBINATIONS USING TABLE 2**Table 4 - Example of Pin Combinations**

This is an example for a 10 pin device with 2-Vdd, 2-Vss, 2-Vcc, 2-input and 2-output pins. The like-named supply pins are metallurgically connected on the die. The sequence number refers to the sequence of pin combinations for stressing.

Sequence Number	Pin Combination	Connect to A	Connect to B	Float Pins
1	1	1st input pin	2-Vdd	all other 7 pins
2	1	2nd input pin	2-Vdd	all other 7 pins
3	1	1st output pin	2-Vdd	all other 7 pins
4	1	2nd output pin	2-Vdd	all other 7 pins
5	1	1st Vcc pin	2-Vdd	all other 7 pins
6	1	2nd Vcc pin	2-Vdd	all other 7 pins
7	1	1st Vss pin	2-Vdd	all other 7 pins
8	1	2nd Vss pin	2-Vdd	all other 7 pins
9–12	2	Repeat 1–4	2-Vss	all other 7 pins
13	2	1st Vcc pin	2-Vss	all other 7 pins
14	2	2nd Vcc pin	2-Vss	all other 7 pins
15	2	1st Vdd pin	2-Vss	all other 7 pins
16	2	2nd Vdd pin	2-Vss	all other 7 pins
17–20	3	Repeat 1–4	2-Vcc	all other 7 pins
21	3	1st Vss pin	2-Vcc	all other 7 pins
22	3	2nd Vss pin	2-Vcc	all other 7 pins
23	3	1st Vdd pin	2-Vcc	all other 7 pins
24	3	2nd Vdd pin	2-Vcc	all other 7 pins
25	4	1st input pin	outputs 1, 2 & input 2	all Vdd, Vss & Vcc pins
26	4	2nd input pin	outputs 1, 2 & input 1	all Vdd, Vss & Vcc pins
27	4	1st output pin	inputs 1, 2 & output 2	all Vdd, Vss & Vcc pins
28	4	2nd output pin	inputs 1, 2 & output 1	all Vdd, Vss & Vcc pins

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ANNEX B – INFORMATIVE - HBM TEST METHOD FLOW CHART



(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-001-2010)

ANNEX C – INFORMATIVE - HBM TEST EQUIPMENT PARASITIC PROPERTIES

C.1 Optional Trailing Pulse Detection Equipment / Apparatus

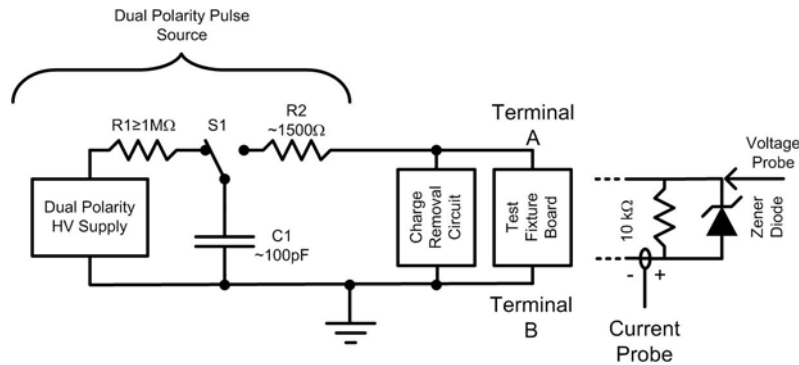


Figure 5: Diagram of Trailing Pulse Measurement Setup

The maximum trailing current pulse level is defined as the maximum peak current level observed through a 10 kilohm test load (current = voltage across test load divided by 10 kilohm) after the normal HBM pulse(s). The time period to be evaluated for after-pulse leakage, is from 0.1 to 1 millisecond after the decay of the HBM current pulse. In the case that a spurious current pulse is observed, begin the 0.1 millisecond measurement point from the start of the spurious current pulse.

The magnitude of the trailing current pulse shall be less than four microamperes when the applied HBM stress voltage is at 4000 volts. This includes both positive and negative polarities. (See Figures 6 and 7 for sample waveforms).

A circuit for measuring the trailing current pulse is shown in Figure 5. The voltage probe shall have input impedance no less than 10 megohm, an input capacitance no larger than 10 picofarad, a bandwidth better than 1 megahertz, and a voltage rating to withstand at least 100 volts. The evaluation load resistance is 10 kilohm in value with tolerance of $\pm 1\%$ and can withstand up to 4000 volts. The Zener diode has a breakdown voltage range from 6 to 15 volts and a power rating from $\frac{1}{4}$ to 1 watt.

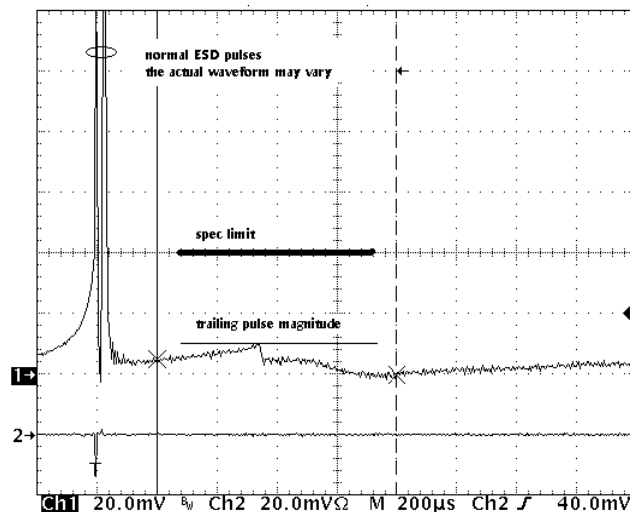


Figure 6: Positive Stress at 4000 Volts

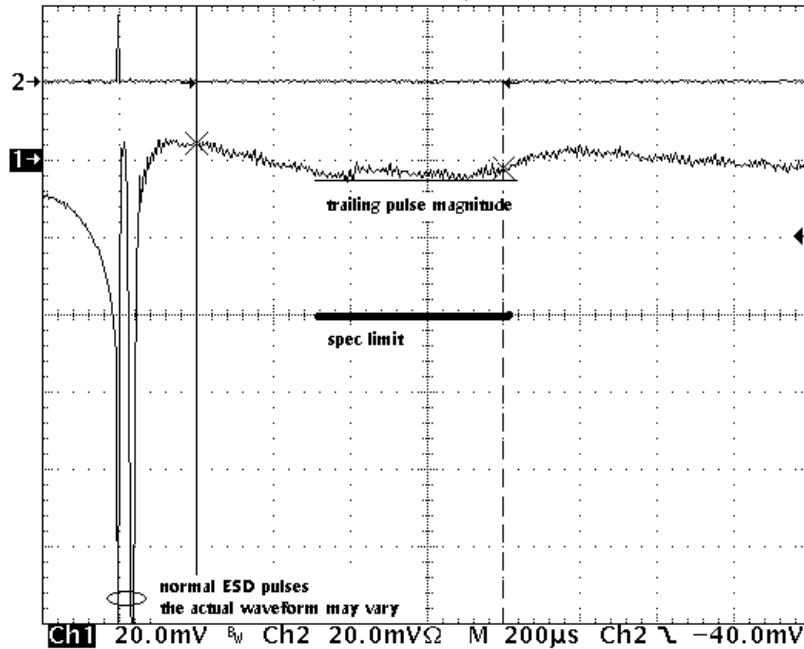


Figure 7: Negative Stress at 4000 Volts

C.2 Optional Pre-Pulse Voltage Rise Test Equipment

HBM events may exhibit a phenomenon which generates a voltage rise at the stressed pin prior to the main HBM current pulse if the pin impedance is high. In some ESD simulators this phenomenon is unrealistically severe and may lead to inconsistent ESD threshold results. The characteristics of this pre-current pulse voltage event depend on the conditions and the environment of the arcing associated with the HBM discharge, the parasitic capacitances of the tester, as well as the pin impedance of the device under test. To determine the magnitude of the resulting voltage rise the following test equipment and apparatus is required. (See Figure 8 for measurement setup).

The worst-case condition will be measured for a low capacitance Zener diode with a voltage in the 8 to 10 volt range. The Zener diode will provide protection for the voltage probe and its low capacitance will not reduce the voltage buildup appreciably. The current transducer on the groundside of the diode is used to trigger an oscilloscope. The voltage probe, connected to a second channel of the oscilloscope, should have high resistance such as a 10 megohm 10X probe. Sample data is shown in Figure 9 for a 9.4 volt Zener diode. The HBM current pulse occurs at time zero and cannot be seen at this time scale. At the time scale of an HBM event, tens to hundreds of nanoseconds, the voltage before the HBM current pulse would appear as a DC voltage across the diode. To measure the voltage across a device the Zener diode is replaced by the device of interest.

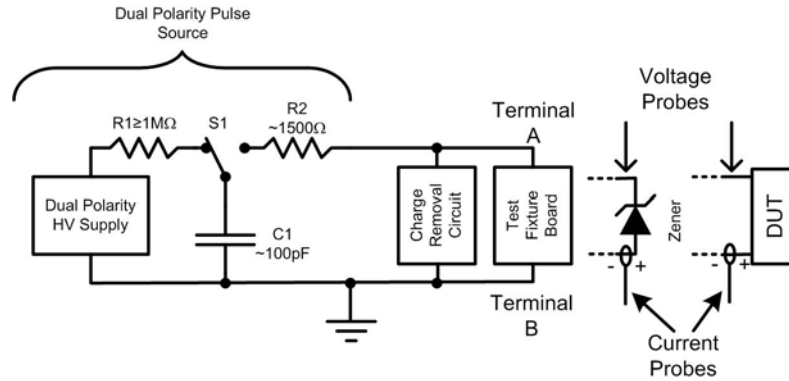


Figure 8: Illustrates Measuring Voltage Before HBM Pulse with a Zener Diode or a Device

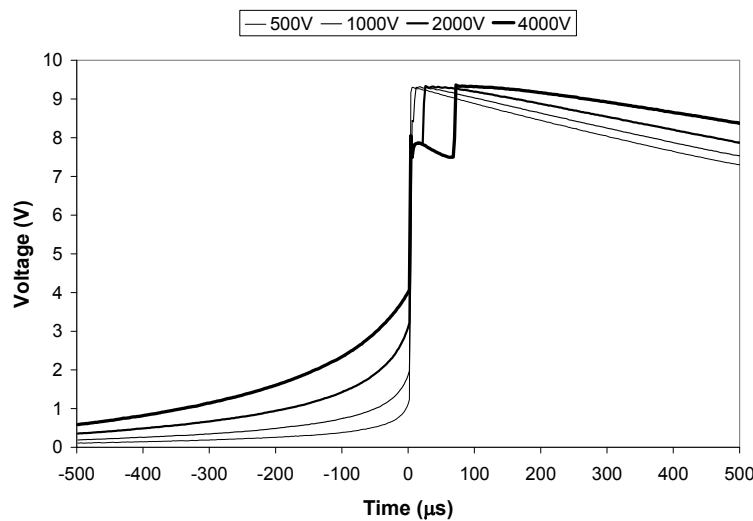


Figure 9: Example Voltage Rise Before the HBM Current Pulse Across a 9.4 Volt Zener Diode

C.3 Open-Relay Tester Capacitance Parasitics

The HBM stressing of a single supply pin is complicated when the pin is part of a group of multiple like-name supply pins (balls) that are shorted together via the DUT (e.g., via a package plane). When the component is placed in the socket only one pin can be connected to Terminal A. The other supply pins are left “floating” as the HBM simulator’s connect relays are opened so the other supply pins do not connect to Terminal A or B.

Recent HBM tester research on package-plane-shortened pins has found that when a single pin is stressed, the other “floating” supply pins act like small capacitors. Since the relays are open, no DC current will flow to ground, but the open-relay capacitors will charge. This parasitic capacitance per pin is quite small (4 – 8 pF/pin) and will vary among HBM simulators. Since each floating pin is placed in parallel, the parasitic capacitance grows as the number of supply pins connected to the power plane increases. This tester parasitic capacitance will be in parallel with the test board capacitance and will have the affect of slowing down the HBM peak current rise time and will reduce the HBM peak currents. All relay matrix HBM simulators have this property.

The impact on HBM test results is difficult to determine as it depends on the sensitivity of the ESD circuits of the supply pins to slow di/dt rise times. For some designs and equipment, the HBM levels may either increase or decrease. If failure levels are lower than expected, the best option is to retest the supply pins on a 2-pin manual tester. If the 2-pin HBM levels are much higher,

then the open-relay capacitance is probably causing the lower HBM failure levels. In some cases, tester channels can be isolated by adding insulators or removing pogo pins from the HBM tester. This effectively “floats” the parallel supply pins. If there is a known problem for a given package, then special test fixture boards can be designed that connect only one supply pin from the socket to the HBM simulator. This modified test fixture board will not wire the floating pins to the HBM simulator, so these pins will not be able to charge up the open-relay capacitors.

Another alternative method that can be used to overcome possible tester parasitic capacitance is the use of the “Alternative Pin Stress Method for Non-Supply Pins” discussed in Section 6.6.

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-001-2010)

ANNEX D – INFORMATIVE - BIBLIOGRAPHY

MIL-STD-883D Test Methods and Procedures for Microelectronics: Method 3015.7 Electrostatic Discharge Sensitivity Classification.

MIL-STD-750C Notice 4: Test Methods for Semiconductor Devices: Method 1020: Electrostatic Discharge Sensitivity Classification.

(This Annex is not part of ESDA/JEDEC Joint Standard ANSI/ESDA/JEDEC JS-001-2010)

ANNEX E – INFORMATIVE - –ESDA/JEDEC JOINT HBM REVISION HISTORY

E.1 Joint Document Summary

This is the initial version of this standard and is a combination of ANSI/ESD STM5.1 and JESD22 – A114F. It is intended to replace these and all previous versions. The merged document contains the essential elements of both documents as outlined in this section.

E.2 Summary by Section

- 1.0 Scope and Purpose** – The scope and purpose of the two documents were merged. A clause declaring the acceptability of data obtained from both previous standards was included.
- 2.0 Referenced Documents** - The previous ESDA and JEDEC methods were referenced. The ESDA and JEDEC Glossaries were referenced.
- 3.0 Definitions** – Definitions from ESDA and JEDEC Glossary of Terms were used as appropriate. New definitions for failure window and package plane were added.
- 4.0 Apparatus and Required Equipment** – This section was re-written. Descriptions of oscilloscope and current transducers were refined. The HBM circuit schematic and description was improved. References to pre-pulse and trailing pulse phenomena were made. Details for mitigating these effects were moved to Annex C.
- 5.0 Stress Test Equipment Qualification And Routine Verification** - This section was completely re-written. Qualification and verification of test fixture boards was largely based on ANSI/ESD STM5.1. Two alternate daily verification procedures were defined. A new section on the determination of ringing was added (5.2.3.3).
- 6.0 Classification Procedure** - The basic procedure for sampling, pin combinations and stressing were the same in both documents. Sections 6.5.2 and 6.6 are special techniques which were adopted in A114F and were under consideration in ANSI/ESD STM5.1 at the time this merged version was created.
- 7.0 Failure Criteria** – No changes. Documents were the same.
- 8.0 Classification Criteria** - No changes. Documents were the same.

Annexes

A – Example of Pin Combinations Using Table 2 – This is the same as the example in ANSI/ESD STM5.1.

B – HBM Test Method Flow Chart – This was modified from flow chart in ANSI/ESD STM5.1 to reflect flow in the merged document.

C - HBM Test Equipment Parasitic Properties – This annex contains information on the “pre-pulse” and “trailing pulse” phenomena and provides optional procedures for mitigation which were contained in both JEDEC and ESDA documents. Tester parasitic information was added.