ESD Association Standard

ANSI/ESD S5.3.1-2009

**ANSI/ESD S5.3.1-2009**

*Revision and Redesignation of ANSI/ESD STM5.3.1-1999*

# *For Electrostatic Discharge Sensitivity Testing –*

# *Charged Device Model (CDM) – Component Level*

***Electrostatic Discharge Association***
***7900 Turin Road, Bldg. 3***
***Rome, NY 13440***

*An American National Standard*
*Approved December 4, 2009*

# *ESD Association Standard for Electrostatic Discharge Sensitivity Testing –*

# *Charged Device Model (CDM) – Component Level*

Approved July 31, 2009
ESD Association

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## FOREWORD

The earliest electrostatic discharge (ESD) test models and standards simulate a charged object approaching a component and discharging through the component. However, with the increasing use of automated component handling systems another potentially destructive discharge mechanism, the charged device model (CDM) becomes increasingly important. In the CDM a component itself becomes charged (e.g., by sliding on a surface (tribocharging) or by electric field induction) and is rapidly discharged (by an ESD event) as it closely approaches a conductive object.

Accurately quantifying the CDM discharge event is very difficult, if not impossible, due to the limitations of the measuring equipment and its influence on the discharge event. The CDM discharge is generally completed in a few nanoseconds, and peak currents of tens of amperes have been observed. The peak current into the component will vary considerably depending on a large number of factors, including package type and parasitics. The typical failure mechanism observed in MOS components for the CDM model is dielectric damage, although other damage has been noted.

The CDM sensitivity of a given component is package dependent. An integrated circuit (IC) chip in a small outline package (SOP) configuration may be more susceptible to CDM damage when compared to a dual-in-line (DIL) package configuration. ICs in thin, small outline packages (TSOP), or pin grid array (PGA) packages typically have the lowest CDM withstand voltage.

Based on results obtained with early CDM testers (not necessarily meeting the waveform requirements of this standard), components with CDM sensitivities of 500 volts or less proved difficult to handle without damage. Components with CDM sensitivities of 1,000 volts or more did not experience major field problems when proper handling techniques were followed. Recent data indicate with proper ESD controls, safe handling of devices with CDM sensitivities of 250V is achieved.

Waveform parameters for the 30 pF verification module may be subject to change in future revisions of this document.

This CDM document does not apply to the socketed discharge model testers.

This document was originally designated ANSI/ESD STM5.3.1-1999 and approved on September 26, 1999. This standard[1] is a revision of ANSI/ESD STM5.3.1-1999 and was approved on July 31, 2009. This standard was prepared by the 5.3.1 (CDM) Device Testing Subcommittee.

[1] ESD Association Standard (S): A precise statement of a set of requirements to be satisfied by a material, product, system or process that also specifies the procedures for determining whether each of the requirements is satisfied.

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**ESD Association Standard for Electrostatic Discharge (ESD) Sensitivity Testing – Charged Device Model (CDM) – Component Level**

## 1.0 SCOPE AND PURPOSE

### 1.1 Scope

This standard establishes the procedure for testing, evaluating and classifying the electrostatic discharge (ESD) sensitivity of components to the defined charged device model (CDM).

### 1.2 Purpose

The purpose of this document is to establish a test method that simulates CDM failures and provides reliable and repeatable results from tester to tester. This will allow accurate comparisons of component CDM ESD sensitivity levels.

## 2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this standard to the extent specified herein:

ESD ADV1.0. ESD Association Glossary of Terms[2]

## 3.0 DEFINITIONS

The following definitions are in addition to those found in the ESD Association's Glossary of Terms:

**Charged Device Model (CDM) Electrostatic Discharge (ESD).** An ESD stress model that approximates the discharge event that occurs when a charged component is quickly discharged to another object at a lower electrostatic potential through a signal pin or terminal.

**Charged Device Model (CDM) Electrostatic Discharge (ESD) Tester.** Equipment (referred to as "tester" in this standard) that simulates the component level CDM ESD event using the non-socketed test method.

**Coaxial Resistive Probe.** A resistor (for example, a 1.0 ohm disk resistor) used to measure the CDM discharge current.

**Field Plate (FP).** A conductive plate used to elevate the potential of the device under test (DUT) by capacitive coupling (see Figure 1).

**Ground Plane (GP).** A conductive plate used to complete the circuitry for grounding / discharging the DUT (see Figure 1).

**Non-contact Mode Discharge.** An air discharge ESD event that is initiated by a probe tip or pogo pin approaching a component pin.

## 4.0 PERSONNEL SAFETY

The procedures and equipment described in this document may expose personnel to hazardous electrical conditions. Users of this document are responsible for selecting equipment that complies with applicable laws, regulatory codes and both external and internal policy. Users are cautioned that this document cannot replace or supersede any requirements for personnel safety.

Ground fault circuit interrupters (GFCI) and other safety protection should be considered wherever personnel might come into contact with electrical sources.

Electrical hazard reduction practices should be exercised and proper grounding instructions for equipment shall be followed.

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[2] ESD Association, 7900 Turin Road, Bldg. 3, Rome, NY 13440-2069; 315-339-6937; FAX: 315-339-6793; www.esda.org

## 5.0 ESD COMPONENT CLASSIFICATIONS

ESD sensitive (ESDS) components are classified according to their ESD withstand voltage using the test procedure described in this standard. The CDM ESDS component classification levels are presented in Table 1.

**Table 1. CDM ESDS Component Classification Levels**

| Class | Voltage Range |
|---|---|
| C1 | < 125 volts |
| C2 | 125 to < 250 volts |
| C3 | 250 to < 500 volts |
| C4 | 500 to < 1,000 volts |
| C5 | 1,000 to < 1,500 volts |
| C6 | 1,500 to < 2,000 volts |
| C7 | ≥ 2,000 volts |

NOTE: Use the "C" prefix to indicate a CDM classification.
NOTE: For voltages above 1,500 Volts, depending on geometry of the device package, corona effects may limit the actual pre-discharge voltage and discharge current.

## 6.0 COMPONENT CHARGING AND DISCHARGING METHODS

Either of the following two methods may be used to raise the component potential for the subsequent CDM discharge:

### 6.1 Direct Charging Method

The component to be tested is placed on the field plate (FP) and charged through the pin which best provides an ohmic connection to the substrate or bulk material of the component, or through all pins simultaneously. The total charging resistance (see Figure 1) shall be at least 100 megohm. Contact to the charging pin(s) shall be established before the voltage is raised. Each pin is discharged one at a time (including power supply pins and ground pins), except the pins connected to the substrate. Re-charge the component after each pin has been discharged.

To prevent component damage, precautions shall be taken to ensure the charging mechanism and component are at ground potential prior to the initial connection. At least one megohm of the charging resistance shall be physically placed close to the charging pin to isolate the effect of any residual charge on the charge up line. It is permissible to leave the charging probe on the charging pin during the discharge cycle, provided the waveform requirements of Section 8.0 are satisfied.

NOTE: The substrate, or bulk material, is typically called Vss, or ground, for NMOS or for n-well (p-substrate) CMOS technologies; and Vcc, or Vdd, for p-well (n-substrate) CMOS technologies. For a charge-pumped substrate (where there is no direct access through an external pin), the Vss or ground pin is still appropriate to use.

***6.1.1*** Multichip modules or other special components (e.g., silicon-on-sapphire, silicon-on-insulator, and hybrids) shall be charged through a common power supply pin to ensure the entire component reaches the charging potential.

NOTE: For multichip modules with no common supply pin, the direct charging method is not recommended.

***6.1.2*** If the process technology is unknown, charge the component through the Vss or ground pin. Make note of the charging pins when reporting the results. Vpp pins shall never be used as charging pins.

***6.1.3*** The Dielectric layer is a non-conductive or insulative material used to form a capacitive circuit between the Field Plate (FP) and the Device Under Test (DUT). The dielectric is specifically useful for CDM when stress testing devices with metallic heat sinks. See Section 6.2 and Section 7.0, Figure 1.

### 6.2 Field-induced Charging Method

Place the component to be tested on the FP. Raise the potential of the component by raising the potential of the FP. Discharge through one pin. Repeat the procedure until all pins are stressed (including all power supply pins: Vdd, Vcc, Vss, Vpp, etc.).

***6.2.1*** The size of the FP (at least seven times larger in area than the size of the component under test) shall be such that the waveform qualification meets the requirement of Section 8.0. The FP should be connected to the power supply or ground through a greater than 100 megohm resistor (see Figure 1).

***6.2.2*** The size of the ground plane (GP) shall be such that it completely covers the entire device during stress testing of any of the pins, with a size margin to allow for fringing fields.

***6.2.3*** The thickness of the dielectric layer covering the FP shall have a maximum thickness of 130 microns (micrometers), as the presence of the dielectric reduces the package capacitance between the component and the FP, which affects the discharge current. Take precautions to ensure components are not charged prior to testing.

### 6.3 Discharging Method

See Informative Annex A for background information on the discharging method (non-contact mode discharge).

## 7.0 REQUIRED EQUIPMENT

### 7.1 CDM ESD Tester

Figure 1 represents the conceptual schematic for test setup to conduct field-induced CDM ESD testing. The CDM ESD tester used within the context of this standard shall meet the waveform characteristics specified in Figures 4 and 5, and Tables 3 and 4. K1 is the switch between charging the FP and grounding the FP.

NOTE: When constructing the test equipment, the parasitics in the charge and discharge paths should be minimized, since the resistance inductance-capacitance (RLC) parasitics in the equipment greatly influence the test results.

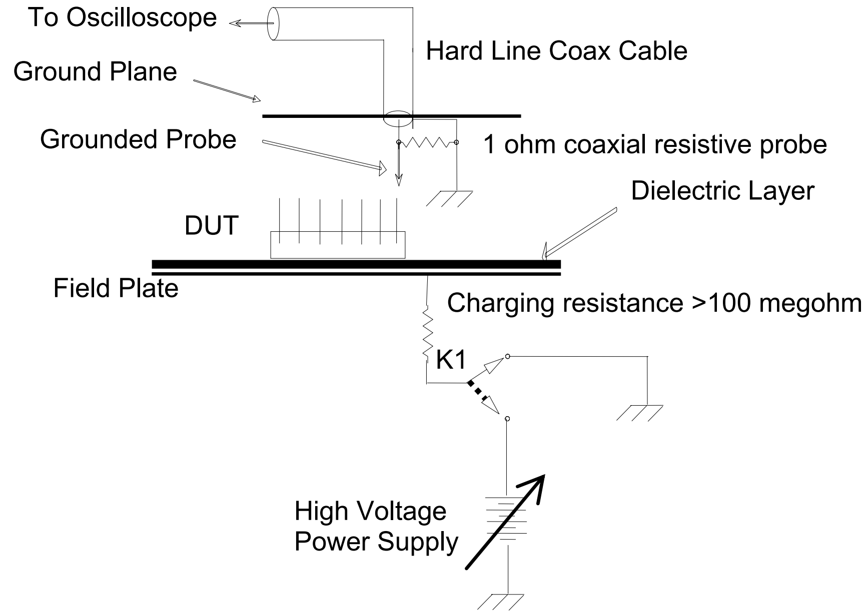


*Figure 1: Conceptual Schematic of the CDM Tester*

## 7.2 Waveform Measurement Equipment

### *7.2.1 Equipment for 3.0 Gigahertz Waveform Measurement*

7.2.1.1 Oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3 decibel (dB)-bandwidth (BW) of at least 3.0 gigahertz (GHz) and ≥ 20 gigasample/sec sampling rate with a nominal 50 ohm input impedance.

NOTE: The BW and the sampling rate will affect the observed waveform. Using different oscilloscopes with different BW (rise times) are permitted only if appropriate filtering (software or hardware) is specified to produce a BW and sampling rate equivalent to that specified in Section 7.2.1.1.

7.2.1.2 Attenuator

Attenuator with a precision of 0.1 dB up to 18.0 GHz, a DC precision of the attenuation factor of 5% and an impedance of 50 ± 3 ohms.

7.2.1.3 Probe

A coaxial resistive probe or inductive current transducer with at least five times the BW of the oscilloscope specified (or 18.0 GHz, which ever is less).

7.2.1.4 Cable Assemblies

Cable assemblies with no more than 0.4 dB loss at frequencies up to 18.0 GHz and impedance of 50 ± 2 ohms.

### *7.2.2 Equipment for 1.0 Gigahertz Waveform Measurement*

7.2.2.1 Oscilloscope

An oscilloscope or transient digitizer with a real-time (single shot) 3dB bandwidth (BW) of at least 1.0 GHz with a nominal 50 ohm input impedance. The sampling rate shall be at least five times the BW of the oscilloscope.

NOTE: The user has an option of using a higher BW oscilloscope and using a rise time filter to reduce the rise time to 1.0 GHz. The resulting BW and sampling shall meet that specified in Section 7.2.2.1.

7.2.2.2 Attenuator

Attenuator with a precision of ± 0.1 dB at five times the BW of what is being measured, a DC precision of the attenuation factor of 5% and an impedance of 50 ± 3 ohms.

7.2.2.3 Probe

A coaxial resistive probe or inductive current transducer with at least five times the BW of the oscilloscope being used.

7.2.2.4 Cable Assemblies

Cable assemblies with no more than 0.1 dB loss at frequencies up to five times the BW of the oscilloscope being used and an impedance of 50 ± 2 ohms.

### *7.2.3 Verification Modules*

Two gold-plated or nickel-plated etched copper disks on single-sided insulative circuit board material. Refer to Informative Annex B for information on the verification modules. The circuit board material can be FR-4 or RF-35. Each disk shall be etched in the center of a square of the insulative material. The larger disk shall have a capacitance of 30 pF ± 5%. The smaller disk shall have a capacitance of 4.0 pF ± 5%. The capacitance is measured with the non-metallized (non-disk) side of the verification modules in intimate contact with the metal surface of the grounded FP. The verification module construction is shown in Figures 6 and 7. Specifications for verification modules are presented in Table 5.

NOTE: The module capacitance shall be measured as specified at 1 MHz. If the modules do not comply with the specified capacitance limits, they cannot be used.

NOTE: The FR-4 (abbreviation for Flame Resistant) material is a dielectric (insulative) material made up of epoxy glass, which absorbs moisture. The dielectric constant of this material determines the capacitance of the module. Since the material is known to be sensitive to moisture, this module should be stored in a low moisture environment when not in use. Conditioning or baking may be used to return the module to an acceptable moisture content level. Failure to follow the storage guidelines may result in waveform parameters (e.g. peak currents) that are outside the required specifications. The RF-35 (abbreviation for Radio Frequency) material is not sensitive to moisture and therefore this material does not need to be stored in a low moisture environment.

NOTE: Since both materials (FR-4 and RF-35) have different properties, the user is responsible for the choice of materials.

### *7.2.4 Capacitance Meter*

Capacitance meter with a resolution of 0.2 pF, a measurement accuracy of 3% and a measurement frequency of 1.0 MHz.

### *7.2.5 Ohmmeter*

The ohmmeter used to measure the resistance of the coaxial resistive probe shall be capable of measuring 1.00 ± 0.01 ohms. Use of Kelvin 4-wire connections is advisable.

## 8.0 PERIODIC EQUIPMENT CALIBRATION, TESTER QUALIFICATION, WAVEFORM RECORDS AND WAVEFORM VERIFICATION REQUIREMENTS

### 8.1 Equipment Calibration

Calibrate all equipment used for tester or waveform verification in accordance with the manufacturer's recommendations, with a maximum of one year between calibrations. This equipment list includes oscilloscope, attenuator, current transducer, coaxial resistive probe,

capacitance meter, and verification module(s) conforming to the requirements of Section 7.2. Calibration shall be traceable to national standards, such as National Institute of Standards and Technology (NIST) in the United States, or international standards.

#### *8.1.1 Capacitance of Verification Modules*

8.1.1.1 Place the non-metallized non-disk (dielectric) side of the 4.0 pF verification module in intimate contact with the metal surface of the grounded FP. Ensure there is no air space between the module and the FP.

8.1.1.2 Measure the capacitance of the module to the grounded FP using the capacitance meter. The capacitance value of the verification module shall be within the value specified in Section 7.2.3.

8.1.1.3 The capacitance can also be measured outside of the CDM tester.

8.1.1.4 Repeat Section 8.1.1.1 using the 30 pF verification module on the grounded FP.

8.1.1.5 Measure the capacitance of the module to the grounded FP using the capacitance meter. The capacitance value of the verification module shall be within the value specified in Section 7.2.3.

NOTE: Caution should be exercised to ensure that during the manufacturing of the disks, they are free from burrs. This is to avoid arcing at the perimeters.

### 8.2 Tester Qualification

Perform the CDM ESD tester qualification as part of the initial acceptance testing and routinely as suggested by the manufacturer. The maximum period between full qualification tests shall be one year. In addition, repeat qualification testing whenever the equipment is serviced in a manner which the manufacturer or user defines as having the potential for modifying discharge current waveforms. The CDM ESD tester qualification procedure is specified in Section 9.1. Periodic waveform verification shall be performed in accordance with Section 8.4.

NOTE: Due to the high cost of waveform measuring equipment, manufacturer certified discharge heads may be used and waveform verification performed using a lower BW monitor as specified in Section 7.2.2.

### 8.3 Tester Waveform Records: New Equipment

Record positive and negative waveforms during the tester initial qualification procedures. Waveform records are required for charge levels as defined in the tester qualification procedure. Retain the waveform records until the next calibration or for the duration specified by internal record-keeping procedures.

### 8.4 Tester Waveform Verification

Verify and record the ESD tester waveforms periodically, using the verification modules defined in Section 7.2.3. The maximum time between verifications shall be one month for equipment that is in use for at least 30 hours per week, or up to three months for testers used less frequently. Verification shall include waveform observations and comparison to waveform records for both positive and negative polarities. See Section 9.2 for the waveform verification procedure.

Dielectric layers, ground planes (ground plates), the coaxial discharging resistor (probe), the distance between the GP and the FP, the verification modules and discharge contacts (e.g., pogo pins) are key elements of the tester construction. Any change to these requires tester waveform verification.

## 9.0 QUALIFICATION AND VERIFICATION PROCEDURES

For the purpose of both the equipment qualification and the waveform verification, the verification modules are treated as components.

### 9.1 CDM ESD Tester Qualification Procedure

CDM ESD tester qualification shall ensure waveform integrity of the discharge current for both positive and negative polarities and each verification module specified in Section 7.2.3. Measure the waveform using the full BW oscilloscope (3.0 GHz), attenuator, current probe or coaxial resistive probe described in Section 7.2.1. Do not use the 1.0 GHz measuring equipment for tester qualification.

***9.1.1*** Clean the verification modules. Avoid skin contact with the modules prior to and during testing. Refer to Informative Annex C for a recommended procedure.

***9.1.2*** Clean tester components to remove any surface contamination that could result in charge loss. Pay particular attention to the discharge probe, charging probe and the FP on which the device is placed. Refer to Informative Annex C for a recommended procedure.

***9.1.3*** Place the 30 pF verification module on the FP, ensuring intimate contact (no air space) between the module and the FP. When a dielectric layer is used for component testing, it shall meet the requirements specified in Section 6.2.3 and shall be present during the qualification procedure.

***9.1.4*** Set the horizontal time scale of the oscilloscope to 0.5 nanoseconds per division. Set the oscilloscope vertical sensitivity and offset, using attenuators if necessary, to cover the center 80% of the full-scale deflection.

***9.1.5*** Change the potential of the module, or FP, to positive 500 volts.

***9.1.6*** Discharge the module with the discharge probe close to the center of the verification module and record the discharge current waveform. All parameters shall be within the limits specified in Figure 4 and Table 3. Record the waveform.

***9.1.7*** Repeat the procedure given in steps 9.1.5 and 9.1.6 at least two more times. Save the record for future verifications. (Record all and save the one closest to the mean for future verification.)

***9.1.8*** Change the potential of the module, or FP, to negative 500 volts. Repeat the procedure given in steps 9.1.6 and 9.1.7.

***9.1.9*** For the 4.0 pF verification module, repeat steps 9.1.4 through 9.1.8 using all the voltage levels in Table 3. If the maximum potential of the tester is lower than 2,000 volts, use that as the maximum. Set the oscilloscope vertical sensitivity and offset, using attenuators if necessary, to cover the center 80% of the full-scale deflection for each voltage level. All parameters shall be within the limits specified in Figure 4 and Table 3. Save these records for future verifications.

***9.1.10*** It is recommended that all waveform records be supplied with the tester for future waveform verification purposes.

**Table 2. CDM ESD Stress Levels**

| Stress Level | Charging Voltage (V) |
|---|---|
| 1 | 125 |
| 2 | 250 |
| 3 | 500 |
| 4 | 1,000 |
| 5 | 1,500 |
| 6 | 2,000 |

### 9.2 Waveform Verification Procedure

Waveform verification shall ensure waveform integrity of the discharge current, as specified in this standard, for both positive and negative polarities, using the small 4.0 pF verification module specified in Section 7.2.3.

If the 1.0 GHz BW measuring equipment will be used for future waveform verification, repeat the CDM ESD tester qualification procedure using the 1.0 GHz BW oscilloscope (see Figure 5 and Table 4). Record the waveforms for future comparison purposes during waveform verification.

***9.2.1*** Clean the 4.0 pF verification module. Avoid skin contact with the module prior to and during testing. Refer to Informative Annex C for a recommended procedure.

***9.2.2*** Clean the tester to remove any surface contamination that could result in charge loss. Pay particular attention to the discharge probe, charging probe and the FP on which the device is placed. Refer to Informative Annex C for a recommended procedure.

***9.2.3*** Place the 4.0 pF verification module on the FP, ensuring intimate contact (no air space) between the module and the FP. When a dielectric layer is used for component testing, it shall meet the requirements specified in Section 6.2.3 and be present during the qualification procedure.

***9.2.4*** Set the horizontal time scale of the oscilloscope to 0.5 nanoseconds per division, and set the vertical sensitivity to allow for approximately 10 amperes full-scale deflection.

***9.2.5*** Change the potential of the module, or FP, to positive 500 volts.

***9.2.6*** Discharge the module and observe the current waveform. All parameters shall be within the limits specified in Figure 4 and Table 3 if the 3.0 GHz waveform measuring equipment is used. If the narrower BW waveform measuring equipment is used, ensure that all parameters are within the limits specified in Figure 5 and Table 4. It is recommended that the waveform parameters be compared to the previous satisfactory verification record.

NOTE: Changes in the shape of the discharge pulse, even though they are within specification, may indicate degradation of the discharge path.

***9.2.7*** Change the potential of the module, or FP, to negative 500 volts. Repeat the procedure given in step 9.2.6.

***9.2.8*** Remove the verification module.

## 10.0 CDM ESDS TESTING REQUIREMENTS AND PROCEDURES

### 10.1 Test Requirements

#### *10.1.1 Handling of Components*

Use ESD prevention procedures before, during and after testing.

#### *10.1.2 ESD Stress Test Temperature*

Stabilize the component to room temperature prior to and during the ESD stress testing period.

#### *10.1.3 Recommended Waveform Check*

At the beginning and end of each shift during which testing is performed, ensure waveform integrity for the discharge head for the 500 volt level of Table 2, for positive and negative polarities, using the 4.0 pF verification module. If the waveforms no longer meet the specified limits (see Figures 4 or 5 and Tables 3 or 4), all test results subsequent to the previous satisfactory check shall be considered invalid. If testing is performed in consecutive shifts, waveform checks at the end of one shift may also serve as the initial checks for the following shift.

#### *10.1.4 Component Static and Dynamic Tests*

Perform full static and dynamic testing to specified component data sheet parameters prior to and following ESD stress testing to determine whether components have failed.

NOTE: While pin leakage current and standby current may be used as a guide in determining the ESD withstand voltage, it is not an adequate criterion of component failure for complex integrated circuits. However, a change in pin leakage or standby current is a sensitive indicator for the onset of damage.

NOTE: Static and dynamic testing immediately following the ESD stressing provides worst-case test data results. With some components, static and dynamic characteristics may be out of specified data sheet limits when tested immediately following ESD stressing, but drift toward acceptable levels with time. If static and dynamic testing is delayed, the component may be improperly classified at a higher ESD withstand voltage.

NOTE: If static and dynamic testing is to be performed at several temperatures, perform the tests first at the lowest temperature, followed by the increasing temperatures in sequence.

### 10.2 CDM Component Classification Testing Procedure

Classify components according to their CDM ESD withstand voltage as shown in Table 1. Stress test the components according to the procedure below. Testing may be initiated at any level desired. If the component fails, continue testing with a new component at a lower voltage until the withstand voltage is determined. If the component passes at the initial level, continue testing following the voltage levels specified in Table 2 until the component fails or the maximum charge voltage is reached. CDM ESD classification testing shall be considered destructive, even if the component does not fail during testing. Smaller voltage level increments may be used to determine withstand voltage if desired.

NOTE: A change in component package, manufacturing processes, design or materials may require component reclassification according to this standard. Even if the same chip is used in a different package, it should be re-classified; no generic qualifications should be allowed.

NOTE: A classification is for a particular die in a particular package with a unique bond-out.

The following procedure shall be used to classify components:

***10.2.1*** Test a minimum of three samples of the component to all specified static and dynamic data sheet parameters.

***10.2.2*** Install the first component and begin testing using a stress level from Table 2.

***10.2.3*** Raise the component potential using either of the methods, as specified in Section 6.0. If the direct charging method of Section 6.1 is used, discharge the pin under test a total of six times (three positive and three negative). If the field-induced charging method of Section 6.2 is used, then follow either the procedure in Section 10.2.3.1.1 or the procedure in Section 10.2.3.1.2. Apply a total of six discharges (three positive and three negative) to each pin. The time between discharges shall be sufficient to allow the component to reach the full stress voltage, with a minimum time between discharges of one second.

*10.2.3.1* When using the field-induced charging method, there are two possible procedures for charging and discharging the DUT: single discharge procedure and dual discharge procedure. Both procedures produce equivalent results.

*10.2.3.1.1* Single Discharge Procedure: The three positive and three negative discharges can be applied with six individual discharges using this sequence of steps producing the sequence of charging / discharging events as illustrated in Figure 2.

a. The field voltage is established by raising the voltage on the FP to the specified stress level.

b. The first discharge is made by lowering the pogo pin to the DUT (see Figure 2).

c. After the discharge, the pogo pin is brought into physical contact with the component pin under test (PUT) to ensure full charge transfer and to provide a conduction path to ground.

d. Then the voltage on the FP is slowly (resistively) returned to zero, which completely removes the charge that was transferred to the DUT during the first CDM discharge.

e. The pogo pin is returned to its starting (separated) position (see Figure 2) before the voltage of the same or opposite polarity is applied to the FP for subsequent discharges.

f. This sequence is repeated six times (3 positive and 3 negative in any order) to obtain the six discharges.

g. Repeat for each pin to be tested.

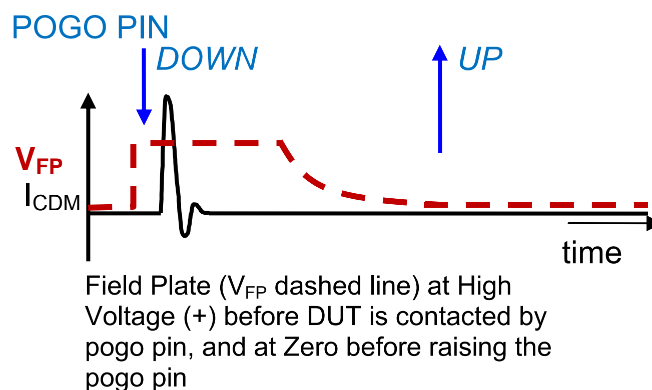


***Figure 2: Single Discharge Procedure (Field charging, $I_{CDM}$ Pulse, and slow discharge)***

*10.2.3.1.2* Dual Discharge Procedure: The three positive and three negative discharges can be applied with three pairs of alternating polarity discharges using this sequence of steps producing the sequence of charging / discharging events as illustrated in Figure 3.

a. The field voltage is established by raising the voltage on the FP to the specified stress level.

b. The first discharge is made by lowering the pogo pin to the DUT (see Figure 3).

c. The pogo pin continues to descend until it makes physical contact with the DUT. This is to ensure full charge transfer and to provide a conduction path to ground.

d. The pogo pin is returned to its starting separated position (see Figure 3), leaving the device with a net charge.

e. The voltage on the FP is slowly (resistively) returned to zero, which completely removes the charge on the field plate. The DUT will still have a net charge.

f. The pogo pin is lowered (the second down arrow to the right in Figure 3) a second time for the second discharge, which will be of opposite polarity and the same magnitude.

g. These steps are repeated three times for a total of three positive and three negative discharges.

h. Repeat for each pin to be tested.

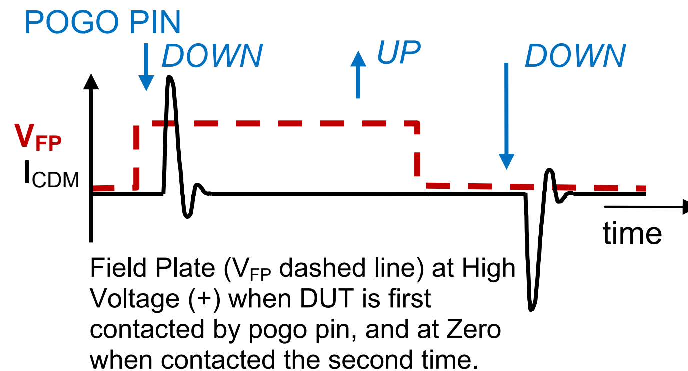


*Figure 3: Dual Discharge Procedure (Field charging, 1st $I_{CDM}$ Pulse, No Field, 2nd $I_{CDM}$ Pulse)*

***10.2.4*** Repeat steps 10.2.2 and 10.2.3 until all three components have been tested. Record the stress level.

***10.2.5*** Test the components to all full static and dynamic data sheet parameters and record the results for each component. Parametric and functional testing shall be performed at room temperature or as specified in the component specification. If testing is required at multiple temperatures, testing shall be performed first at the lowest temperature followed by the increasing temperatures in sequence.

If all the components pass the specified data sheet parameters, repeat steps 10.2.3 through 10.2.5, using the next higher stress level of Table 2.

***10.2.6*** If one or more components fail, repeat the ESD stress test using three new components starting at the next lower stress level. If the components continue to fail, decrease the stress voltage until level one is reached. If any additional failures are observed at level one, stop all testing at this level.

***10.2.7*** As an alternative, three new components may be used at each stress level of Table 2. Separate components may also be used for each polarity and pin. Document and report the sample size and test plan.

## 11.0 CLASSIFICATION CRITERIA

The component classification is the highest ESD stress voltage level (both positive and negative polarities) at which a sample of at least three components has passed full static and dynamic data sheet parameters following ESD testing.

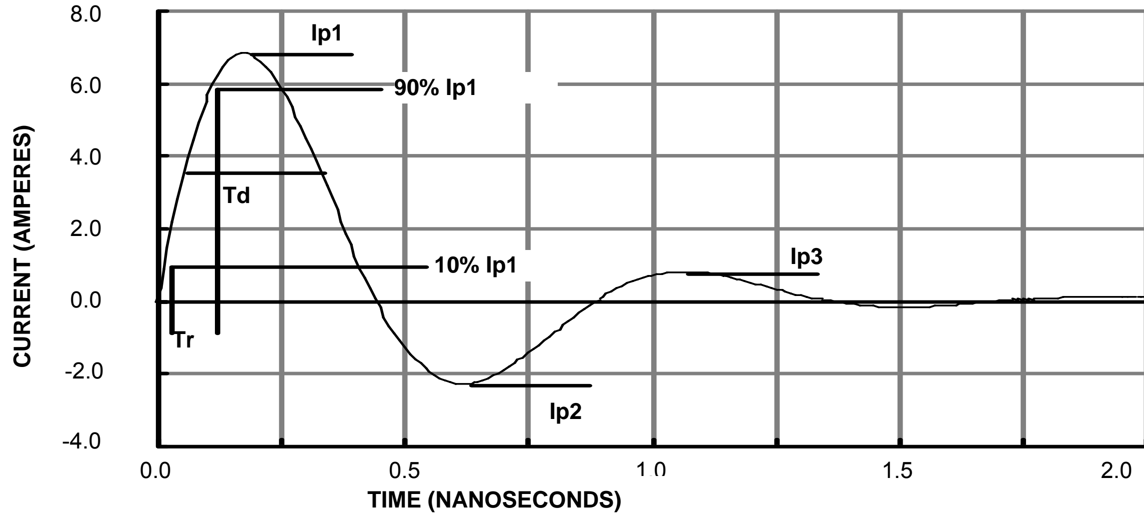


*Figure 4: CDM ESD Waveform for the Verification Modules Using a 3.0 Gigahertz Bandwidth Measurement System*

NOTE: For the positive polarity: $Ip_2$ is the second peak, the undershoot negative peak; $Ip_3$ is the third peak, the overshoot positive peak. For the negative polarity: $Ip_2$ is the second peak, the overshoot positive peak; $Ip_3$ is the third peak, the undershoot negative peak.

**Table 3. Waveform Requirements Using the 3.0 GHz Bandwidth Scope**

| Charge Voltage Volts ± 5% | Symbol | 4.0 pF Verification Module Amperes ± 20% | 30 pF Verification Module Amperes ± 20% |
|---|---|---|---|
| 125 | $Ip_1$ | 1.90 | — |
| 250 | $Ip_1$ | 3.75 | — |
| 500 | $Ip_1$ | 7.50 | 18.0 |
| 1,000 | $Ip_1$ | 15.0 | — |
| 1,500 | $Ip_1$ | 22.5 | — |
| 2,000 | $Ip_1$ | 30.0 | — |
| **Parameter** | **Symbol** | **4.0 pF Verification Module (All voltages)** | **30 pF Verification Module (500 volts only)** |
| Rise Time | $t_r$ (ps) | < 200 ps | < 250 ps |
| Full Width at Half Height | $t_d$ (ps) | < 400 ps | < 700 ps |
| Max. 2nd peak | $Ip_2$ | < 50% $Ip_1$ | < 50% $Ip_1$ |
| Max. 3rd Peak | $Ip_3$ | < 25% $Ip_1$ | < 25% $Ip_1$ |

NOTE: Caution: Many CDM testers use a coaxial 1.0 ohm resistor probe to measure the current. In such a setup, one measures the voltage across the coaxial resistor. This voltage read-out can be translated to a current read-out by dividing the voltage by the resistance value of the coaxial resistor. Therefore, it is important to use the actual resistance value and not an assumed value of 1.0 ohm.

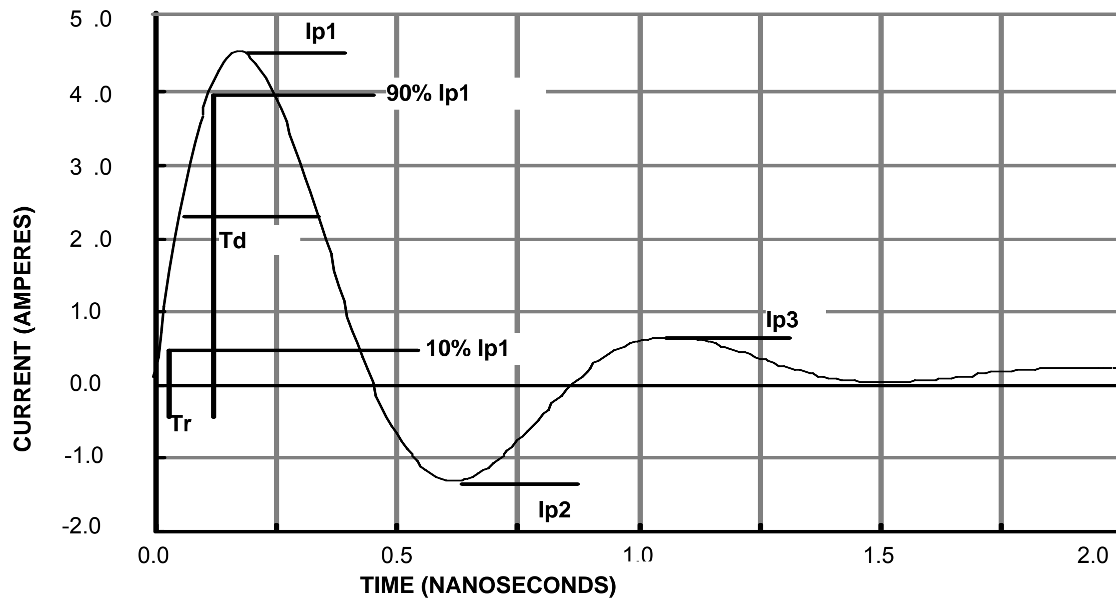


*Figure 5: CDM ESD Waveform for the Verification Modules Using the 1.0 Gigahertz Bandwidth Measurement System*

NOTE: For the positive polarity: $Ip_2$ is the second peak, the undershoot negative peak; $Ip_3$ is the third peak, the overshoot positive peak. For the negative polarity: $Ip_2$ is the second peak, the overshoot positive peak; $Ip_3$ is the third peak, the undershoot negative peak.

**Table 4. Waveform Requirements Using the 1.0 GHz Bandwidth Scope**

| Charge Voltage Volts ± 5% | Symbol | 4.0 pF Verification Module Amperes ± 20% | 30 pF Verification Module Amperes ± 20% |
|---|---|---|---|
| 125 | $Ip_1$ | 1.13 | — |
| 250 | $Ip_1$ | 2.25 | — |
| 500 | $Ip_1$ | 4.50 | 14.0 |
| 1,000 | $Ip_1$ | 9.00 | — |
| 1,500 | $Ip_1$ | 13.5 | — |
| 2,000 | $Ip_1$ | 18.0 | — |
| **Parameter** | **Symbol** | **4.0 pF Verification Module (All Voltages)** | **30 pF Verification Module (500 volts only)** |
| Rise Time | $t_r$ (ps) | < 400 ps | < 400 ps |
| Full Width at Half Height | $t_d$ (ps) | < 600 ps | < 1,000 ps |
| Max 2nd Peak | $Ip_2$ | < 50% $Ip_1$ | < 50% $Ip_1$ |
| Max 3rd Peak | $Ip_3$ | < 25% $Ip_1$ | < 25% $Ip_1$ |

NOTE: Caution: Many CDM testers use a coaxial 1.0 ohm resistor probe to measure the current. In such a setup, one measures the voltage across the coaxial resistor. This voltage read-out can be translated to a current read-out by dividing the voltage by the resistance value of the coaxial resistor. Therefore, it is important to use the actual resistance value and not an assumed value of 1.0 ohm.

(This annex is not part of ESD Association Standard ANSI/ESD S5.3.1-2009)

## ANNEX A (INFORMATIVE) – DISCHARGE TEST METHOD GUIDANCE

### Non-contact Mode Discharge

Air discharge attempts to simulate the charged device model (CDM) event as it would naturally occur in the environment. The discharge actually occurs in air as a grounded object approaches the pin of a charged device. The characteristics of this discharge – breakdown voltage, peak current, wave shape, etc. are determined by a number of factors including air pressure and movement, humidity, electrode shapes, how fast the electrodes are approaching each other, and cleanliness. Because of the difficulty in controlling all of these factors, reproducibility and repeatability of tests is difficult. These tend to alter the discharge characteristics, making replication in a test environment difficult. Some testers overcome the humidity and pressure issues by creating a controlled local environment using a dry inert gas such as nitrogen or clean, dry air.

Frequent cleaning or replacement of the discharge electrode, and cleaning of the component pins before testing, can help alleviate the contamination issues.

A variation in peak current of up to 20% from discharge to discharge is reasonable for non-contact mode discharges. The effect of the variation can be minimized by using statistical control methods after collecting the data.

The major advantages of the non-contact mode discharge technique are that it truly represents the natural discharge conditions and minimizes the parasitic circuit elements.

The major disadvantages are an inability to ensure discharges to a chosen pin when testing components with very close pin spacing, and difficulty in reproducing discharge events within close tolerances.

(This annex is not part of ESD Association Standard ANSI/ESD S5.3.1-2009)

## ANNEX B (INFORMATIVE) – VERIFICATION MODULE PHYSICAL AND ELECTRICAL CHARACTERISTICS

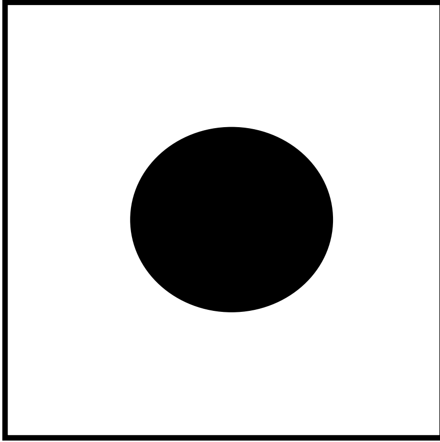

*Figure 6: The 30 pF Verification Module with Large Metallic Disk*

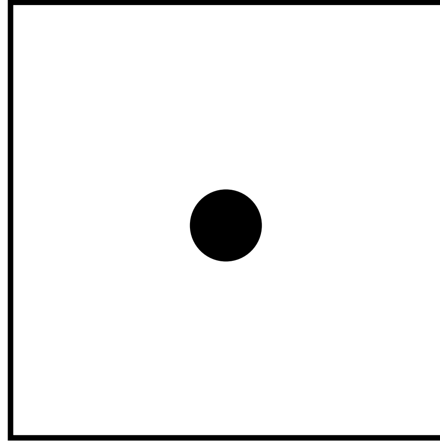

*Figure 7: The 4.0 pF Verification Module with Small Metallic Disk*

NOTE: The physical dimensions given below are meant to be a guide. The final capacitances of the verification modules are to be measured using a capacitance meter as described in Section 8.1.1.

NOTE: Changes to the materials' dielectric constant will change the required dimensions if the specified capacitances are to be maintained.

**Table 5. Specification for Verification Modules**

| Disk Dielectric Material (Size) | FR-4 Small | FR-4 Large | RF-35 Small | RF-35 Large |
|---|---|---|---|---|
| Approximate Dielectric Constant | 4.70 | 4.70 | 3.50 | 3.50 |
| Disk Diameter (mm) | 9.50 | 26.00 | 9.80 | 26.93 |
| Dielectric Thickness (mm) | 0.80 | 0.80 | 0.584 | 0.584 |
| Disk Capacitance (pF) | 4.0 | 30 | 4.0 | 30 |
| Dielectric Square – Minimum Size (mm) | 30 x 30 | 30 x 30 | 30 x 30 | 30 x 30 |

NOTE: The gold-plated or nickel-plated etched copper disks are centered on one side of the dielectric material.

(This annex is not part of ESD Association Standard ANSI/ESD S5.3.1-2009)

## ANNEX C (INFORMATIVE) – RECOMMENDED COMPONENT / VERIFICATION MODULE HANDLING AND TESTER CLEANING GUIDELINES

To avoid charge loss in verification modules during charged device model (CDM) evaluation, the verification modules should be cleaned with isopropanol (isopropyl alcohol, IPA) using a procedure approved by the local safety organization. Components should then be handled only by vacuum tweezers, personnel wearing finger cots or equivalent, or plastic tweezers that have been neutralized by holding in an ionized air stream.

The tester should be cleaned periodically with isopropanol to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe (or pogo pin), charging probe or field plate (FP) on which the device is placed.

NOTE: Cleaning with isopropyl alcohol may leave the surface moist for some period of time after the cleaning. The moisture may provide an unintended leakage path if present during the test. It is important to dry all surfaces after cleaning either by allowing sufficient time for the surfaces to dry or using forced air flow to evaporate the moisture.

(This annex is not part of ESD Association Standard ANSI/ESD S5.3.1-2009)

## ANNEX D (INFORMATIVE) - ANSI/ESD S5.3.1-2009 REVISION HISTORY

1. Foreword: Changed “Waveform parameters for the 30 pF verification module should be used for guidance only, and may be subject to change in future revisions of this document” to “Waveform parameters for the 30 pF verification module may be subject to change in future revisions of this document”. “This CDM document does not apply to the socketed discharge model (SDM) testers” was added.

2. Section 3.0: Definitions.
    a. The definitions were alphabetized.
    b. The following definitions were added: coaxial resistive probe, field plate (FP) and ground plane.
    c. Replaced megaohm with megohm.
    d. The following definitions were removed as they are referenced in the ESDA Glossary: Component Failure, Electrostatic Discharge Sensitivity (ESDS) and ESD Withstand Voltage.

3. Section 4.0: Personnel Safety Section was added (so all subsequent numbered section numbers are one greater than 1999 version, and items 4-10 below refer to the 2009 version section numbers).

4. Section 5 below Table 1.
    a. The second note (suffix codes: c = contact mode ; n = non-contact mode. (For example: C4n = CDM, class 4, non-contact mode.)) was completely removed. We do not address contact mode in this document.

5. Section 6.0: Component Charging and Discharging Methods.
    a. Added new section 6.1.3 Dielectric Layer Explanation.
    b. Added the following to Section 6.2: “The FP should be connected to the power supply or ground through a greater than 100 megohm resistor.” The section is now divided into subsections (6.2.1, 6.2.2 etc) for this version.

6. Section 7.0. Required Equipment.
    a. Added new Figure 1 - Conceptual Schematic of the CDM Simulator
    b. Section 7.1: The first sentence was switched with the second sentence, hence the second sentence is now the first. The words “and Tables 3 and 4” were added at the end of the paragraph to correlate with Figures 4 and 5 respectively.
    c. Added new note reference in Section 7.2.1.1.
    d. Section 7.2.1.2: Changed “at 18 GHz” to “up to 18 GHz”.
    e. Section 7.2.2: Removed the word “User” in the section heading to make it consistent with the heading of section 7.2.1.
    f. Section 7.2.2: A general improvement to descriptions (BW, sampling, etc) of oscilloscopes, attenuators, coaxial resistive probe, inductive current transducer, cable assemblies, and rise time filters.
    g. Section 7.2.3: In the second note the words “with extremely low moisture absorption” were removed and the clarification/definition of FR4 (abbreviation for Flame Resistant), and RF-35 (abbreviation for Radio Frequency) were added.
    h. Section 7.2.5: The word “The” was removed from the heading for consistency. The Ohmmeter and the use of Kelvin 4-wire connections are added.

7. Section 8.1.1: Updated to include measurement of capacitance. This is to be done “inside or outside” of CDM tester.

8. Section 8.4: The following paragraph was added to the section as a second paragraph. "Dielectric layers, Ground Planes (ground plates), the coaxial discharging resistor (probe) the distance between the GP and the FP, the verification modules and discharge contacts (e.g., pogo pins) are key elements of the tester construction. Any change to these requires tester waveform verification".

9. Section 9.0: Qualification and Verification Procedures. The quoted sentence below was changed from being part of the section 9.2.6 to being a note below the section "Changes in the shape of the discharge pulse, even though they are within specification, may indicate degradation of the discharge path".

10. Section 10.2:
    a. The following note was added: "a qualification is for a particular die in a particular package with a unique bond-out."
    b. Section 10.2.3 now has a subsection: 10.2.3.1 (field-induced charging method), which has been split into 2 further subsections to differentiate between the procedures for Single Discharge (10.2.3.1.1) and Dual Discharge (10.2.3.1.2).

11. Section 11: Classification Criteria:
    a. The old Figure 2 (CDM waveform) is now Figure 4.
    b. The table below Figure 4 is now Table 3.
    c. The old Figure 3 is now Figure 5.
    d. The table below Figure 5 is now Table 4.

12. Figure 2 and Figure 3 were added to represent the single Discharge and the dual Discharge Procedures.

13. Changed to using the decimal (4.0, 1.0 etc) in all cases to be consistent.

14. The Annexes now have a distinct difference between Normative (needed) and Informative (informational) and Annex replaced the term Appendix.

15. Annex A (Informative): Was Appendix 1.
    a. Figures 4 and 5 are now Figures 6 and 7.
    b. There is a new Table 5 below Figures 6 and 7 showing the specifications associated with the Verification modules.

16. Annex B (Informative): Was Appendix 2.
    a. The contact mode discharge has been removed. We do not address it in this document.

17. Annex C (Informative): Was Appendix 3.
    a. A note has been added to address the issue of a dry surface after cleaning with IPA (isopropyl alcohol).

18. Annex D (Informative): Revision History was added for this 2009 version.