ESD Association Standard

ANSI/ESD S5.2-2009

ANSI/ESD S5.2-2009

Revision and Redesignation of ANSI/ESD STM5.2-1999

For Electrostatic Discharge Sensitivity Testing –

Machine Model (MM) – Component Level

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

An American National Standard
Approved January 6, 2010

ESD Association Standard for Electrostatic Discharge Sensitivity Testing – Machine Model (MM) – Component Level

Approved September 16, 2009
ESD Association

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Published by:

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

Printed in the United States of America

ISBN: 1-58537-178-5

(This foreword is not part of ESD Association Standard ANSI/ESD S5.2-2009)

FOREWORD

This document defines a method that simulates an electrostatic discharge (ESD) event occurring from a low resistance source. Component damage caused by the machine model (MM) test is often similar to that caused by the human body model (HBM) test, but occurs at a significantly lower voltage. Other forms of ESD-related component damage, such as that induced by the charged device model (CDM), may result in a different failure signature for some components.

Requirements for HBM and CDM testing are contained in the ESD Association Standards ANSI/ESD STM5.1 and ANSI/ESD S5.3.1, respectively.

Users of this standard[1] should understand that the data obtained when classifying components does not necessarily mean that the components will be unaffected if subjected to a lower level actual ESD. This standard is intended to minimize test data correlation problems due to variations between testers.

This document was originally designated ESD S5.2-1994 and approved on June 22, 1994. ANSI/ESD STM5.2-1999 was a revision, re-designation of ESD S5.2-1994 and was approved on May 16, 1999. ANSI/ESD S5.2-2009 is a revision, re-designation of ANSI/ESD STM5.2-1999 and was approved on September 16, 2009.

[1] ESD Association Standard (S): A precise statement of a set of requirements to be satisfied by a material, product, system or process that also specifies the procedures for determining whether each of the requirements is satisfied.

At the time ANSI/ESD S5.2-2009 was prepared, the 5.2 Device Testing (MM) Subcommittee had the following members:

Leo G. Henry, Chair
ESD & TLP Consultants

Robert Ashton ON Semiconductor	Jon Barth Barth Electronics, Inc.	Michael Chaine Micron Technology, Inc.
Marcel Dekker MASER Engineering BV	Marti Farris Intel Corporation	Reinhold Gaertner Infineon Technologies AG
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Alan Righter Analog Devices	Masanori Sawada Hanwa Electronic	Mirko Scholz IMEC
Steven H.Voldman Dr. Steven H. Voldman, LLC	Scott Ward Texas Instruments	Terry Welsher Dangelmayer Associates

The following individuals contributed significantly to the development of ANSI/ESD S5.2-2009:

David Tremouilles
IMEC

At the time ANSI/ESD STM5.2-1999 was prepared, the 5.2 (MM) Device Testing Subcommittee had the following members:

Mark Kelly, Chair
Delphi Delco Electronics Systems

Jon Barth Barth Electronics	Karlheinz Bock IMEC	Bob Carey Lucent Technologies
Mike Chaine Micron Technology	Ira Cohen Intel Corporation	Louis DeChiaro Lucent Technologies
Tom Diep Texas Instruments	Marti Farris Intel Corporation	Bernard Hall Oryx Instruments Corp.
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Satoshi Isofuku Tokyo Electronics Trading Co.	Tom Meuse Thermo-Voltek/KeyTek	John Mick Visteon Automotive Systems
Girish Shah Visteon Automotive Systems		Koen Verhaege Sarnoff Corporation

The following individuals made significant contributions to ANSI/ESD STM5.2-1999:

Les Avery Sarnoff Corporation	Colin Hatchard Thermo-Voltek/KeyTek	Paul Phillips Verifier Systems
Stuart Schwartz Ford Microelectronics	Michael Stevens Motorola	Sam Twerefore Ford Microelectronics
Joseph Veltri Digital Equipment Corp.		Terry Welsher Lucent Technologies

TABLE OF CONTENTS

ANNEXES

TABLES

FIGURES

ESD Association Standard for Electrostatic Discharge (ESD) Sensitivity Testing – Machine Model (MM) – Component Level

1.0 SCOPE AND PURPOSE

1.1 Scope

This document establishes the procedure for testing, evaluating, and classifying the electrostatic discharge (ESD) sensitivity of components to the defined machine model (MM).

1.1.1 Existing Data

Data previously generated with testers meeting all waveform criteria of this standard shall be considered valid test data.

1.2 Purpose

The purpose of this document is to establish a test method that will replicate MM failures and provide reliable, repeatable results from tester to tester, regardless of component type. Repeatable data will allow accurate comparisons of MM ESD sensitivity levels.

2.0 REFERENCED PUBLICATIONS

Unless otherwise specified, the following documents of the latest issue, revision or amendment, form a part of this standard to the extent specified herein:

ESD ADV1.0, ESD Association Glossary of Terms[2]

ANSI/ESD STM5.1, Human Body Model (HBM) – Component Level[2]

3.0 DEFINITIONS

The terms used in the body of this document are in accordance with the definitions found in ESD ADV1.0, ESD Association's Glossary of Terms available for complimentary download at http://www.esda.org/keydownloads.html.

4.0 PERSONNEL SAFETY

The procedures and equipment described in this document may expose personnel to hazardous electrical conditions. Users of this document are responsible for selecting equipment that complies with applicable laws, regulatory codes, and both external and internal policy. Users are cautioned that this document cannot replace or supersede any requirements for personnel safety.

Ground fault circuit interrupters (GFCI) and other safety protection should be considered wherever personnel might come into contact with electrical sources.

Electrical hazard reduction practices should be exercised and proper grounding instructions for equipment shall be followed.

5.0 MM ESDS COMPONENT CLASSIFICATION

Electrostatic Discharge Sensitive (ESDS) components are classified according to their MM ESD withstand voltage, regardless of polarity. The MM ESDS component classification levels are shown in Table 1.

[2] ESD Association, 7900 Turin Road, Bldg. 3, Rome, NY, 13440; Ph: 315-339-6937; FAX: 315-339-6793; www.esda.org

Table 1. MM ESDS Component Classification Levels

Class	Voltage Range (Volts)
M1A	< 25
M1B	25 to < 50
M1C	50 to < 100
M2	100 to < 200
M3	200 to < 400
M4	≥ 400

NOTE: Use the "M" prefix to indicate an MM classification.

6.0 REQUIRED EQUIPMENT

6.1 MM ESD Tester

An acceptable tester is composed of equipment meeting the requirements of this standard (schematically represented in Figure 1 and producing pulses meeting the waveform characteristics represented in Figures 2 and 3 and specified in Tables 4 and 5).

6.2 Waveform Verification Equipment

Equipment capable of verifying the pulse waveforms defined in this standard includes, but is not limited to, an oscilloscope, two evaluation loads, and a current transducer.

6.2.1 Oscilloscope

Oscilloscope requirements:

a. Minimum sensitivity of 100 milliamperes per major division (typically 1 cm [0.4 inches]) when used in conjunction with the current transducer specified in Section 6.2.3.
b. Minimum single shot bandwidth of 350 megahertz.
c. Minimum writing rate of one major division per nanosecond.

6.2.2 Evaluation Loads

Two evaluation loads are necessary to verify tester functionality:

Load a: A solid 18 to 24 American Wire Gauge (AWG) (0.81 to 0.21 mm^2 cross section) tinned copper shorting wire, not longer than 75 mm (3 inches) in length.

Load b: A 500 ohm ± 1%, 1000 volt, low inductance resistor (Caddock Industries type MG 714 or equivalent).

The lead length of both evaluation loads should be as short as possible. The wire should span the distance from the reference pin to any other pin on the test socket while passing through the current transducer.

6.2.3 Current Transducer

Current transducer requirements:

a. Minimum bandwidth of 200 megahertz.
b. Peak pulse capability of 12 amperes.
c. Rise time of less than one nanosecond.
d. Capable of accepting at least a solid 24 AWG wire.

e. Provide an output voltage per milliampere as required in Section 6.2.1.a (usually 1 to 5 millivolt per milliampere).

A Tektronix CT-2 or equivalent with a maximum cable length of one meter meets these requirements.

7.0 EQUIPMENT, WAVEFORM, AND QUALIFICATION REQUIREMENTS

7.1 Equipment Calibration

Periodically calibrate all equipment used to evaluate the tester in accordance with the manufacturers' recommendation. This includes the oscilloscope, current transducer, and high voltage resistor load. Maximum time between calibrations shall be one year. Calibration shall be traceable to national standards, such as the National Institute of Standards and Technology (NIST) in the United States, or to international standards.

7.2 Tester Qualification and Requalification

Perform tester qualification procedures as part of the acceptance testing when the ESD tester is delivered. Refer to the manufacturers' recommendations for acceptance testing procedures. Perform requalification (in accordance with Section 8.2) following repairs or servicing that could affect the waveform. The maximum time between full requalification tests shall be one year. Retain all waveform records for the life of the tester, or for the duration specified by internal record keeping procedures.

7.3 Test Fixture Board Qualification

Perform the test fixture board qualification procedure in accordance with Section 8.3 on all new test fixture boards and any existing boards not previously checked.

The waveform check is required for positive clamp sockets each time the test fixture board is changed. The waveform check is recommended for all other socket types. Refer to Section 8.1 for waveform capture procedures.

7.4 Daily Tester Functionality Check

Verify the ESD tester functionality at least once per shift (Section 8.4). Longer periods between tester checks may be used if no changes in waveforms are observed for several consecutive checks. However, if the waveforms no longer meet the specified limits, all ESD stress tests subsequent to the previous satisfactory waveform check shall be considered invalid.

NOTE: If ESD stress testing is performed on consecutive shifts, tester checks at the end of one shift may also serve as the initial check for the following shift.

8.0 QUALIFICATION AND VERIFICATION PROCEDURES

8.1 Waveform Capture Procedure

Use the following procedure to verify the waveforms:

NOTE: This procedure applies to both single pulse and multiple pulse generation circuits.

8.1.1 The reference pin pair is defined as the pin pair with the shortest and the longest path to the pulse generation circuit. If the tester has more than one pulse generation circuit, a reference pin pair is defined for each pulse generating circuit. This information is typically supplied by the test fixture board designer or manufacturer.

Alternatively, the reference pin pair(s) previously identified during HBM testing may be used. Refer to ANSI/ESD STM5.1.

8.1.2 To capture a waveform using a shorting wire, connect the pin with the shortest wiring path to Terminal B, the ground connection. Place the shorting wire through the current transducer, as close to Terminal B as practical, observing the polarity shown in Figure 1. Connect the other end of the wire to the pin to be tested. This pin is referred to as Terminal A. If the tester has more than one pulse generation circuit, every pulse generating circuit is to be tested individually as a Terminal A connection.

NOTE: For non-positive clamp sockets, attach the shorting wire to the wiring of the test fixture board between the socket pins connected to Terminals A and B. The connection points shall be as close as possible to the test socket pins.

8.1.3 To capture a waveform using the 500 ohm resistor, replace the shorting wire with the resistor. Refer to Figure 1 to determine placement of the resistor in relation to the current transducer.

8.2 Tester Qualification and Requalification Procedure

Use the following procedure for qualification and requalification of the tester:

8.2.1 Test the high voltage discharge path and all associated circuitry (sometimes referred to as Self Test and VI Test) according to the equipment manufacturers' procedures. If more than one pulse generation circuit is used, all high voltage discharge paths are to be tested.

8.2.2 If the equipment has test point capture location(s), capture a waveform from the high voltage pulse generators at each location. Refer to the tester manufacturer manual for procedures.

8.2.3 Using the shorting wire and an applied voltage of 100, 200 and 400 volts, record positive and negative waveforms on each reference pin pair and any other pins recommended by the equipment manufacturer. Verify the waveforms meet the specifications in Figure 2 and Table 4.

8.2.4 To test for spurious pulses; set the horizontal time scale of the oscilloscope to 1 ms per division. Using the shorting wire, initiate a pulse, and verify that any spurious pulse is less than 15% of the amplitude of the main pulse.

8.2.5 Using the 500 ohm resistor and an applied voltage of ± 400 volts, record waveforms for each reference pin pair. Verify the waveforms meet the specifications in Figure 3 and Table 5.

8.3 Test Fixture Board Qualification Procedure

Use the following procedure for qualification of test fixture boards:

8.3.1 Verify electrical continuity for all pins on the test fixture board.

8.3.2 Capture a waveform for each reference pin pair and any other pin combinations recommended by the manufacturer of each socket on the board using the shorting wire and a ± 400 volt pulse. Verify the waveforms meet the specifications in Figure 2 and Table 4.

8.3.3 Capture a waveform on each reference pin pair using the 500 ohm resistor. Use an applied voltage of ± 400 volts. Verify the waveforms meet the specifications in Figure 3 and Table 5.

8.4 Daily Tester Functionality Check Procedure

Use the following procedure to verify tester functionality:

8.4.1 Test the high voltage discharge path and all associated circuitry at the beginning of each day during which ESD stress testing is performed. Use the tester manufacturers' recommended procedure. If any failure is detected, do not perform testing with the sockets that use the defective discharge paths. Repair the tester and then requalify it in accordance with Section 8.2.

8.4.2 Verify the waveform integrity at least once per shift. If necessary, remove the test fixture board being used, and replace with a positive clamp socket test fixture board to facilitate waveform measurements. Verify the waveform using the shorting wire at ± 400 volts, or the stress level to be tested. If the tester has more than one pulse generation circuit, then the waveform from every pulse generation circuit is to be verified.

9.0 MM TESTING REQUIREMENTS

Perform ESD stress testing at room temperature in accordance with the procedure below. It is permissible to use any voltage level in Table 2 as the starting stress level. Additional stress levels to those in Table 2 may be used (e.g. the additional voltages in Table 1). Three new components may be used at each voltage level and/or pin combination if desired. This will eliminate any possible step stress hardening effects and reduce the possibility of early failure due to cumulative stress on power pins. If three new components are used at each voltage level, it is recommended not to skip any stress level missing possible ESD vulnerability windows. Classify components according to their MM ESD withstand voltage.

ESD classification testing shall be considered destructive to the component, even if no component failure occurs.

Table 2. MM ESD Stress Levels

Stress Level	Equivalent Charging (±) Voltage Vp (volt)
1A	25
1B	50
1C	100
2	200
3	400

9.1 Component Handling

Use ESD damage prevention procedures when handling components before, during and after testing.

9.2 Component Static and Dynamic Tests

To determine whether components have failed, perform static and dynamic testing to all data sheet parameters before and after ESD testing. Pin leakage current may only be used as a guide in determining the component ESD withstand voltage. It is not sufficient, especially for complex integrated circuits, to use pin leakage as the only criterion for component failure.

9.3 Test Temperature

Stabilize the component at room temperature prior to and during the ESD stress testing period.

9.4 Sample Size

A minimum of three components is required for each stress level of the test.

9.5 Pin Combinations

The pin combinations to be used for ESD stressing of all integrated circuit components are given in Table 3. Pin combination (n) is the total number of pin combinations. This varies from component to component depending on the number of power pin groups with the same name.

Vps(i) in Table 3, is any set of like-named power supply or ground pins (e.g. Vcc, Vss, Vdd, analog GND, digital GND, etc.) which are metallically connected (within 2 ohms) on the chip or within the package. Like-named pins that are resistively connected via the chip substrate or wells, or are electrically isolated from each other (more than 2 ohms), are considered separate sets for the purpose of these tests. For example, if two pins are labeled Vcc, but are not metallically connected (within 2 ohms) on the chip or within the package, they shall be treated as distinct and separate Vps(i) sets. Only those pins which supply current to, or interface to other pins, shall be considered to be power pins.

Pins such as Vcc, Vdd, GND, Vss, Vee, +Vs, and -Vs are considered power supply pins. These pins supply current to input and output buffers in such a way as to interface closely with the environment through other pins.

Pins such as offset adjust, compensation, clocks, controls, address, data, Vref, no connects (NC), and input and output pins (I/Os) are considered non-power supply pins. For example; a programming power pin, usually called Vpp, shall be considered to be a non-power supply pin because it does not supply current to, or interface with, any other pins and is not a diode drop away from any non-power pins.

For further clarification on pin combinations see the example in Annex A.

9.5.1 Pin combinations for discrete components and component arrays (including both passive and active components) shall be all possible pin pair combinations (one pin to Terminal A, another to Terminal B) regardless of pin function.

10.0 MM ESD STRESS TESTING PROCEDURE

Test a minimum of three samples of the component to all specified static and dynamic data sheet parameters.

10.1 Determine the starting stress voltage level from Table 2. Select the first pin combination to be tested as stated in Section 9.5.

10.2 Apply three positive and three negative pulses to the component. The interval between pulses shall be at least 1 second. Repeat this process using all other pin combinations specified in Section 9.5.

Table 3. Pin Combinations for all Digital, Analog, and Hybrid Integrated Circuit Components

Pin Combination Set	Connect Individually to Terminal A (Stress)	Connect to Terminal B (Ground)	Floating Pins (Unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	Vps(1) [First power pin(s)]	All pins except pin under test (PUT) and Vps(1) [First power pin(s)]
2	All pins one at a time, except the pin(s) connected to Terminal B	Vps(2) [Second power pin(s)]	All pins except PUT and Vps(2) [Second power pin(s)]
i	All pins one at a time, except the pin(s) connected to Terminal B	Vps(i) [ith power pin(s)] [1,2, ...i]	All pins except PUT and Vps(i)
n-1	All pins one at a time, except the pin(s) connected to Terminal B	Vps(n-1)	All pins except PUT and Vps(n-1)
N	All non-Vps(i) pins, one at a time	All other non-Vps(i) pins, except the pin connected to Terminal A	All Vps(i) pins

10.3 Test the components to full static and dynamic data sheet parameters and record the results for each component. Perform parametric and functional testing at room temperature. If testing is required at multiple temperatures, perform testing at the lowest temperature first.

10.4 If all three components pass the specified data sheet parameters, repeat Sections 10.1 through 10.3, using the next higher stress level of Table 2. Three new components may be used at each voltage level or pin combination if desired.

10.5 If one or more components fail, repeat the ESD stress test using three new components starting at the next lower stress level. If the components continue to fail, decrease the stress voltage until level 1A is reached. If any additional failures are observed at level 1A stop all testing at this level.

11.0 CLASSIFICATION CRITERIA

11.1 Classify the component to the highest passing MM ESD stress voltage level from Table 1, at which all three components pass full static and dynamic data sheet parameters following ESD testing.

12.0 ESD TESTER SCHEMATIC AND WAVEFORM PARAMETERS

Machine Model Simulator (Tester)

An acceptable tester is composed of equipment meeting the requirements of this standard (schematically represented in Figure 1 and producing pulses meeting the waveform characteristics represented in Figures 2 and 3 and specified in Tables 4 and 5).

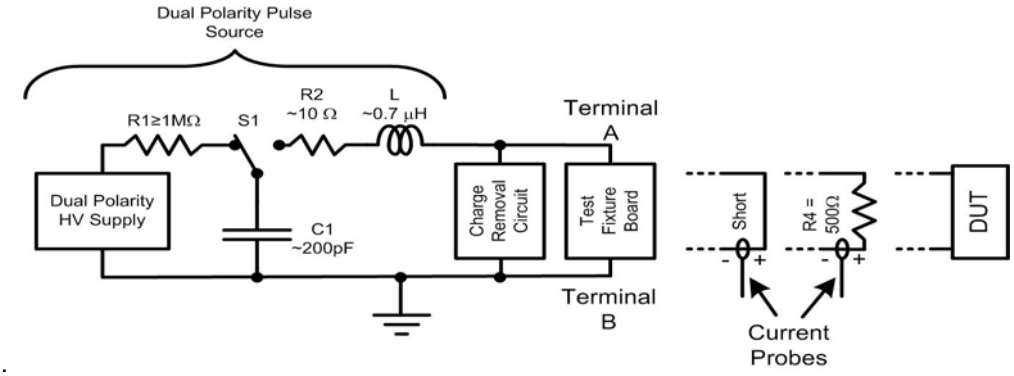

Figure 1: Simplified MM Simulator Circuit with Loads

1. The current transducers are specified in 6.2.3.
2. The evaluation loads (short and the R4-500 ohm resistor) are specified in 6.2.2.
3. Reversal of Terminals A and B to achieve dual polarity performance is not permitted.
4. The charge removal circuit ensures a slow discharge of the device, thus avoiding the possibility of a charged device model discharge. A simple example is a 10 kilohm or larger resistor (possibly in series with a switch) in parallel with the test fixture board.
5. The Dual Polarity Pulse Source shall be designed to avoid recharge transients and double pulses.
6. Stacking of DUT socket adapters (piggybacking or the insertion of secondary sockets into the main test socket) is allowed only if the secondary socket waveform meets the requirements of the standard defined in Table 1.
7. Component values are nominal.

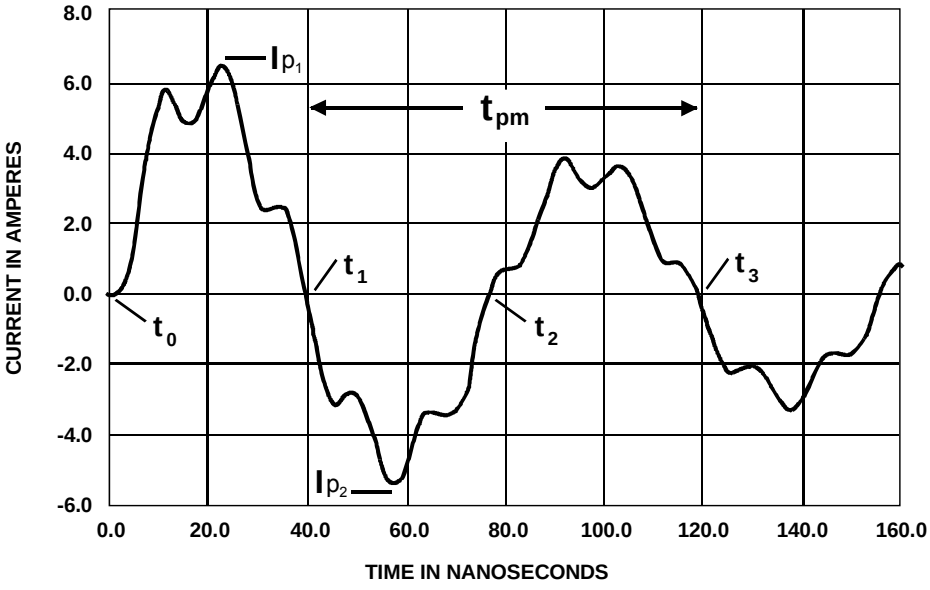

Figure 2: Current Waveform through a Shorting Wire for a 400 volt Discharge

Requirements:

1. The current pulse through a shorting wire shall meet the following characteristics:

Table 4. Characteristics Parameters of Waveform through a Short Circuit

Parameter	Parameter Value		
	Socket Pin Count = 1 to 40 pins	**Socket Pin Count = 41 to 128 pins**	**Socket Pin Count = 129 to 256+ pins (see note b)**
I_{p1} for 25 volt stress (ampere)	0.44 ± 20%	0.44 ± 20%	0.44 ± 20%
I_{p1} for 50 volt stress (ampere)	0.88 ± 20%	0.88 ± 20%	0.88 ± 20%
I_{p1} for 100 volt stress (ampere)	1.75 ± 10%	1.75 ± 15%	1.75 ± 20%
I_{p1} for 200 volt stress (ampere)	3.5 ± 10%	3.5 ± 15%	3.5 ± 20%
I_{p1} for 400 volt stress (ampere)	7.0 ± 10%	7.0 ± 15%	7.0 ± 20%
I_{p2} as % of I_{p1}, **for all stress levels**	67% to 90%	67% to 90%	67% to 90%
t_{pm} (nanoseconds) (see note a)	66 to 90	66 to 90	66 to 90

NOTE a: t_{pm} is the period of the major pulse measured between the first zero crossing point, t_1, and the third zero crossing point, t_3.

NOTE b: For larger pin count devices, the 20% tolerance may cause miscorrelation between testers, particularly if stress steps smaller than those specified in Table 2 are used.

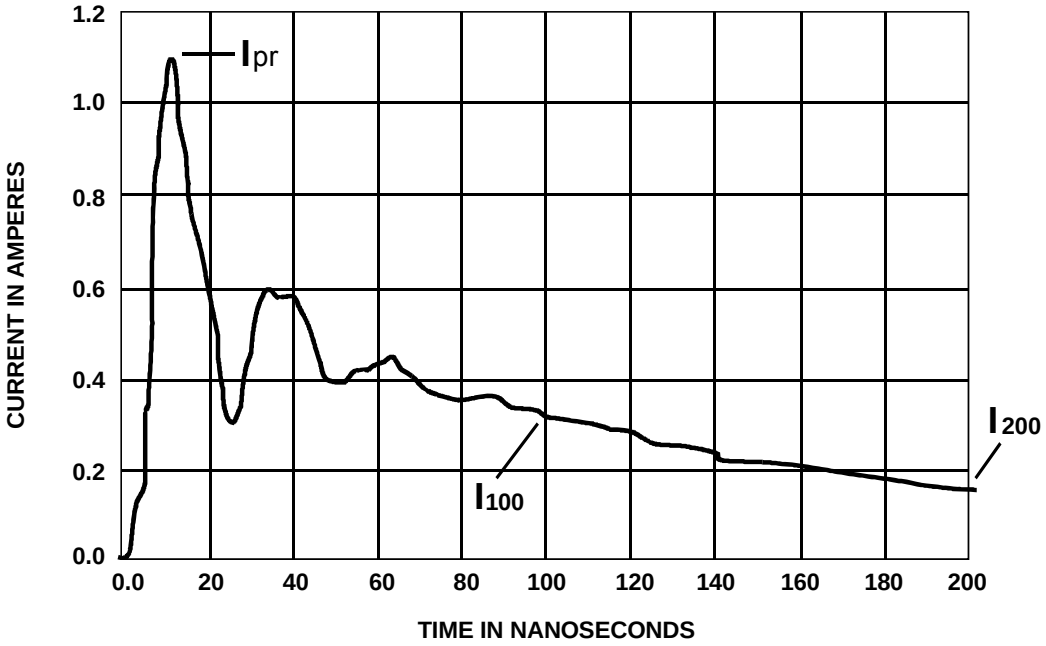

Figure 3: Current Waveform through a 500 ohm Resistor for a 400 volt Discharge

Requirements:

1. The current pulse through a 500 ohm resistor shall meet the following characteristics for a ± 400 volt discharge:

Table 5. Characteristics Parameters of Waveform Through a 500 ohm Resistor

Parameter	Parameter Value
I_{PR} (ampere)	0.85 – 1.2
I_{100} (ampere)	0.23 – 0.40
I_{200} as % of measured I_{100}	30 – 55%

(This annex is not part of ESD Association Standard ANSI/ESD S5.2-2009)

ANNEX A (INFORMATIVE) – EXAMPLE OF PIN COMBINATIONS

The following example is intended to clarify the pin combinations given in Table 3. The example is for a 10 pin device with 2-Vdd, 2-Vss, 2-Vcc, 2-input, and 2-output pins. It is assumed that the like-named power supply pins are metallically connected (within 2 ohms) on the chip or within the package. If not, each should be treated as an individual power supply pin. Power supply and ground pins include Vdd, Vcc, Vss, Gnd, +Vs, -Vs, etc. as defined in Section 9.5. Pins such as offset adjust, compensation, clock, control, address, data, Vref, no connect (NC), and input and output (I/O) shall be considered non-power supply pins. For each pin combination sequence, follow the procedure established in Section 9. The sequence number in the table below refers to the order of pin combinations for stressing.

Table 6. Example of Pin Combinations

Sequence Number	Pin Combination Set	Connect to Terminal A (Stress)	Connect to Terminal B (Ground)	Float Pins (Unconnected)
1	1	1st input pin	2-Vdd	All other 7 pins
2	1	2nd input pin	2-Vdd	All other 7 pins
3	1	1st output pin	2-Vdd	All other 7 pins
4	1	2nd output pin	2-Vdd	All other 7 pins
5	1	1st Vcc pin	2-Vdd	All other 7 pins
6	1	2nd Vcc pin	2-Vdd	All other 7 pins
7	1	1st Vss pin	2-Vdd	All other 7 pins
8	1	2nd Vss pin	2-Vdd	All other 7 pins
9–12	2	Repeat 1–4	2-Vss	All other 7 pins
13	2	1st Vcc pin	2-Vss	All other 7 pins
14	2	2nd Vcc pin	2-Vss	All other 7 pins
15	2	1st Vdd pin	2-Vss	All other 7 pins
16	2	2nd Vdd pin	2-Vss	All other 7 pins
17–20	3	Repeat 1–4	2-Vcc	All other 7 pins
21	3	1st Vss pin	2-Vcc	All other 7 pins
22	3	2nd Vss pin	2-Vcc	All other 7 pins
23	3	1st Vdd pin	2-Vcc	All other 7 pins
24	3	2nd Vdd pin	2-Vcc	All other 7 pins
25	4	1st input pin	output 1, 2 and input 2	all Vdd, Vss and Vcc pins
26	4	2nd input pin	output 1, 2 and input 1	all Vdd, Vss and Vcc pins
27	4	1st output pin	input 1,2 and output 2	all Vdd, Vss and Vcc pins
28	4	2nd output pin	input 1, 2 and output 1	all Vdd, Vss and Vcc pins

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ANNEX B (INFORMATIVE) – MM ANSI/ESD S5.2 PROCEDURE FLOW

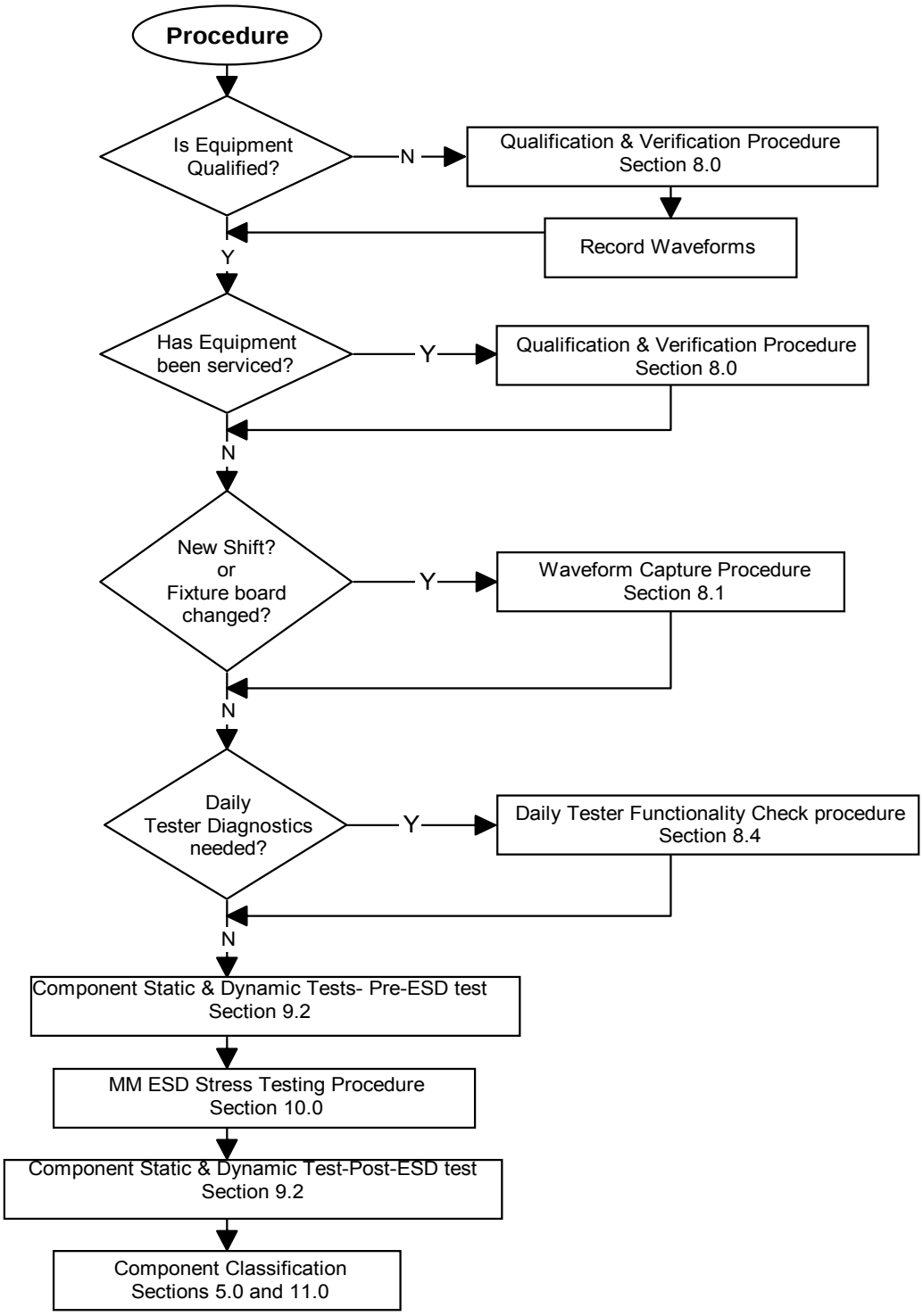

Figure 4: MM ANSI/ESD S5.2 Procedure Flow

(This annex is not part of ESD Association Standard ANSI/ESD S5.2-2009)

ANNEX C (INFORMATIVE) – ANSI/ESD S5.2-2009 REVISION HISTORY

1. New MM definitions added: Active components; Discrete component; $I_{p1,}$ I_{p2}; I_{pr}; No connect (NC) Pin; Passive Components; Pulse Generation Circuit; and Spurious Current Pulses. All definitions previously appearing in ADV1.0 ESD Glossary have been removed and the remaining definitions were alphabetized.

2. Required equipment changes:
   a. Section 6.1 – was reworded to include "and specified in Tables 4 and 5."
   b. Section 6.2.2a – was reworded to include "(3 inches)".
   c. Section 6.2.2b – "Sputtered Film" requirement was removed because resistors which are not sputtered are also eligible and can be used.
   d. Section 6.2.2 - Note 1 was deleted.
   e. Section 6.2.3a – the minimum bandwidth of 250 MHz was changed to "200 megahertz."
   f. Section 6.2.3b – the peak pulse capability of 15 amperes was changed to "12 amperes."
   g. Section 6.2.3 – the statement "A CT-2 probe or equivalent should be used if testing above 800 volts" was removed.

3. Equipment, Waveform and Qualification Requirement changes:
   a. Section 7.4 – the Section title "Daily Tester Functionality Check" was added.

4. Qualification and Verification procedure changes:
   a. Section 8.1 – Addition of a new Note: "This procedure applies to both single pulse and multiple pulse generation circuits."
   b. Section 8.1.1 – Added statements (i) "Alternatively, the reference pin pair(s) previously identified during HBM testing may be used. Refer to ANSI / ESD STM5.1." (ii) "If the tester has more than one pulse generation circuit, a reference pin pair is defined for each pulse generating circuit."
   c. Section 8.1.2 – Note number was removed. Added statement: "If the tester has more than one pulse generation circuit, every pulse generating circuit is to be tested individually as a Terminal A connection."
   d. Section 8.2.1 – Added statement "If more than one pulse generation circuit is used, all high voltage discharge paths are to be tested."
   e. Section 8.2.2 – The full sentence reworded to include the words "at each location".
   f. Section 8.2.3 – reworded to include "and Table 4".
   g. Section 8.3.2 – reworded to include "and Table 4".
   h. Section 8.3.3 – reworded to include "and Table 5".

5. Table 1 changes :
   a. The class M1 has been redefined from "<100 V" to 3 subclasses: "M1A <25;" "M1B 25 to <50," and "M1C 50 to <100."

6. Table 2 changes:
   a. Changed original Table 3 to Table 2 and Table 2 was placed after Section 8.0.
   b. The class 1 has been redefined from one stress level of "100 volts" to 3 subclasses: "1A = 25 volts," "1B = 50 volts," and "1C = 100 volts."
   c. All references to table in text changed accordingly.

7. Table 3 changes:
   a. Changed original Table 2 to Table 3 and the said Table 3 was placed after Section 9.2.
   b. All references to table in text changed accordingly.

8. ESD Tester Schematic and Waveform Parameter changes:
   a. Section 11.0 added before Figure 1.
   b. Figure 2 Table changes:
      i. The table included is now identified as “Table 4: Characteristics Parameters of Waveform through a Short Circuit.”
      ii. Two rows were added to include I_p (current) data for 25 volts and 50 volts.
      iii. Note 4 and Note 5 were changed to “Note 5 and Note 6.”
   c. Figure 3 changes:
      i. The table included is now identified as “Table 5: Characteristics Parameters of Waveform through a 500 ohm resistor.”
      ii. The requirements were moved after Table 5.
      iii. The parameter value for I_{100} was changed from 0.26 – 0.32 to 0.23 – 0.40 amperes.
      iv. The parameter value for I_{200} was changed from 35 – 45% to 30 – 55% of I_{100}.

9. Annex A changes:
   a. The title “Appendix A” was reworded as “Annex A (Informative).”

10. Annex B changes:
    a. The title “Appendix B” was reworded as “Annex B (Informative).”

11. Annex C (Informative) Revision History was added.