ESD Association Standard Practice

ANSI/ESD SP5.3.2-2008

ANSI/ESD SP5.3.2-2008

Reaffirmation of ANSI/ESD SP5.3.2-2004

For the Protection of Electrostatic Discharge Susceptible Items

Sensitivity Testing Socketed Device Model (SDM) Component Level

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

An American National Standard
Approved December 15, 2008

ESD Association Standard Practice for the Protection of Electrostatic Discharge Susceptible Items –

Sensitivity Testing Socketed Device Model (SDM) Component Level

Approved September 7, 2008
ESD Association

CAUTION NOTICE

Electrostatic Discharge Association (ESDA) standards and publications are designed to serve the public interest by eliminating misunderstandings between manufacturers and purchasers, facilitating the interchangeability and improvement of products and assisting the purchaser in selecting and obtaining the proper product for his particular needs. The existence of such standards and publications shall not in any respect preclude any member or non-member of the Association from manufacturing or selling products not conforming to such standards and publications. Nor shall the fact that a standard or publication is published by the Association preclude its voluntary use by non-members of the Association whether the document is to be used either domestically or internationally. Recommended standards and publications are adopted by the ESDA in accordance with the ANSI Patent policy.

Interpretation of ESDA Standards: The interpretation of standards in-so-far as it may relate to a specific product or manufacturer is a proper matter for the individual company concerned and cannot be undertaken by any person acting for the ESDA. The ESDA Standards Chairman may make comments limited to an explanation or clarification of the technical language or provisions in a standard, but not related to its application to specific products and manufacterers. No other person is authorized to comment on behalf of the ESDA on any ESDA Standard.

DISCLAIMER OF WARRANTIES

THE CONTENTS OF ESDA'S STANDARDS AND PUBLICATIONS ARE PROVIDED "AS-IS," AND ESDA MAKES NO REPRESENTATIONS OR WARRANTIES, EXPRESS OR IMPLIED, OF ANY KIND WITH RESPECT TO SUCH CONTENTS. ESDA DISCLAIMS ALL REPRESENTATIONS AND WARRANTIES, INCLUDING WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY, FITNESS FOR PARTICULAR PURPOSE OR USE, TITLE AND NON-INFRINGEMENT.

DISCLAIMER OF GUARANTY

ESDA STANDARDS AND PUBLICATIONS ARE CONSIDERED TECHNICALLY SOUND AT THE TIME THEY ARE APPROVED FOR PUBLICATION. THEY ARE NOT A SUBSTITUTE FOR A PRODUCT SELLER'S OR USER'S OWN JUDGEMENT WITH RESPECT TO ANY PARTICULAR PRODUCT DISCUSSED, AND ESDA DOES NOT UNDERTAKE TO GUARANTY THE PERFORMANCE OF ANY INDIVIDUAL MANUFACTURERS' PRODUCTS BY VIRTUE OF SUCH STANDARDS OR PUBLICATIONS. THUS, ESDA EXPRESSLY DISLAIMS ANY RESPONSIBILITY FOR DAMAGES ARISING FROM THE USE, APPLICATION, OR RELIANCE BY OTHERS ON THE INFORMATION CONTAINED IN THESE STANDARDS OR PUBLICATIONS.

LIMITATION ON ESDA's LIABILITY

NEITHER ESDA, NOR ITS MEMBERS, OFFICERS, EMPLOYEES OR OTHER REPRESENTATIVES WILL BE LIABLE FOR DAMAGES ARISING OUT OF OR IN CONNECTION WITH THE USE OR MISUSE OF ESDA STANDARDS OR PUBLICATIONS, EVEN IF ADVISED OF THE POSSIBILITY THEROF. THIS IS A COMPREHENSIVE LIMITATION OF LIABILITY THAT APPLIES TO ALL DAMAGES OF ANY KIND, INCLUDING WITHOUT LIMITATION, LOSS OF DATA, INCOME OR PROFIT, LOSS OF OR DAMAGE TO PROPERTY AND CLAIMS OF THIRD PARTIES.

Published by:

Electrostatic Discharge Association
7900 Turin Road, Bldg. 3
Rome, NY 13440

Printed in the United States of America

ISBN: 1-58537-162-9

(This foreword is not part of ESD Association Standard Practice ANSI/ESD SP5.3.2-2008)

FOREWORD

This Standard Practice provides a procedure for generating a "Socketed Device Model" (SDM) test on a component integrated circuit (IC) device. The term SDM was derived from Socketed Charge Device Model (S-CDM) test method, which refers to the Charged Device Model (CDM) tests of an IC device mounted in a socket. This is in contrast to the CDM test method, STM5.3.1, where the IC device is tested while in a dead-bug (or pins facing up) configuration and the package is in intimate contact with a charge plate during the charging process.

In this procedure, the device under test (DUT), socket, test fixture board, HV relays and other parts of the test simulator are charged and discharged during the test. The charge is uniquely stored in a distributive network of parasitic capacitance and inductance elements starting from the high voltage supply, the high voltage and ground relays, the pogo pins, the test fixture board, the socket and the DUT. Consequently, the discharge currents through the pin under test represent the charge stored in the IC device and the SDM test simulator's distributive network. The peak current will vary as the trace length on the test fixture board changes. The discharge waveform is unique for the 32-pin DIP and 512-pin PGA Test Fixture Boards (TFB). **Using a different size TFB will produce different waveform parameters including I_{p1}, t_r , t_d and t_z.**

ESD test equipment designed to meet this Standard Practice generates repeatable fast transient over damped current discharge waveforms for a given stress voltage. This unique test system provides valuable information regarding the relative ESD sensitivity of an IC device to a sub-nanosecond rise time and high current discharge from the pin of a socketed device to a ground potential.

This SDM Standard Practice provides guidance for setting up, verifying functionality, and performing SDM testing on components. If the methods defined in this Standard Practice are followed, then the data collected can be used to compare test results from identically designed and verified SDM test simulators.

This standard was originally designated ANSI/ESD SP5.3.2-2004 and was approved on February 22, 2004. Standard Practice ANSI/ESD SP5.3.2-2008 is a reaffirmation of ANSI/ESD SP5.3.2-2004 and was approved on September 7, 2008. Both documents were prepared by the 5.3.2 Device Testing (SDM) Subcommittee.

At the time the 2004 version was prepared, the 5.3.2 Device Testing (SDM) Subcommittee had the following members:

Michael Chaine, Chair
Micron Technologies

John Barth
Barth Electronics, Inc.

Tilo Brodbeck
Infineon Technologies

Marti Farris
Intel Corporation

Horst Gieser
Fraunhofer IZM

Evan Grund
Oryx Corporation

Leo G. Henry
ESD TLP Consultants/Testing

Mark Kelly
Delphi Electronics & Safety

Natarajan Mahadeva Iyer
IMEC

Tom Meuse
Thermo Electron Corporation

Larry Ting
Texas Instruments, Inc.

The following individuals contributed to the development of ANSI/ESD SP5.3.2-2004:

Hugh Hyatt
Hyger Physics, Inc.

Mike Hopkins
Thermo Electron Corporation

TABLE OF CONTENTS

1.0 PURPOSE AND SCOPE

1.1 Purpose

The purpose of this draft standard practice is to define a method to verify the correct operational state of the test simulator, describe a procedure for measuring acceptable SDM discharge waveforms, determine critical waveform parameters and their acceptable values, and provide recommendations for device testing and ESD stressing levels.

1.2 Scope

This standard practice defines a method on how to perform component level Socketed Device Model ESD tests and how to verify the operational state of the ESD simulator test equipment. This document is a Standard Practice and therefore does not provide any device classification guidelines.

2.0 REFERENCES

Unless otherwise specified, the following documents of the latest issue, revision or amendment form a part of this standard to the extent specified herein:

ESD ADV. 1.0 Glossary of Terms[1]

ESD STM5.3.1 – Charged Device Model (non-Socketed) [1]

ESD – TR8-00 - SDM Technical Report[1]

3.0 DEFINITIONS

The following definitions are in addition to those found in ESD ADV 1.0, ESD Association's Glossary of Terms:

I_{p1} : The peak current measured at the absolute maximum of the discharge current waveform (Figure 2).

Positive Clamp Socket: A positive clamp test socket is a zero insertion force (ZIF) socket with a clamping mechanism. This type of socket allows the shorting wire to be easily clamped into the socket. Examples are dual in-line package (DIP) and pin grid array (PGA) ZIF sockets.

Socketed Device Model: An ESD discharge event through a relay matrix network approximating the charge stored in an IC component, socket and test simulator's RLC parasitic elements to ground or to lower electrostatic potential.

Socketed Device Model (SDM) Tester: ESD test equipment designed to stress components that use the Socketed Device Model.

Socketed Discharge: An ESD event is initiated by a relay. The relay is connected to the component pin via a single pogo pin and a trace on the test fixture board while the component is placed in a socket.

t_r : The rise time of the first peak current I_{p1} measured between the times 10% and of 90% of I_{p1} (Figure 2).

t_d : The time duration of the first positive half cycle of the current waveform measured between the first time the current waveform crosses the current axis and the second time the waveform crosses the current axis (Figure 2).

[1] ESD Association, 7900 Turin Rd., Bldg. 3, Rome, NY 13440, www.esda.org

t_z : The duration time of the SDM pulse width measured at 75% of I_{p1}.

4.0 REQUIRED EQUIPMENT

4.1 Socketed Device Model (SDM) ESD Tester

4.2 Waveform Verification Equipment

4.2.1 Oscilloscope requirements:

4.2.1.1. Minimum single shot bandwidth of 1.0 GHz.
4.2.1.2. Minimum sampling rate of 5GS/s.
4.2.1.3. If oscilloscopes with different bandwidths are used, see Appendix A for guidance.

4.2.2 Short Module

The short module is a 14-pin plastic DIP package with all pins internally shorted together (Thermo KeyTek, part #67-005-925-00, or equivalent). A 22-gauge wire extends through the top of the package to connect from the shorted pins to a pin in the socket. The wire should be as short as possible and should be positioned at either pin 1 or pin 14 of the module, depending on the module being used, to minimize the inductive effects on the discharge waveform (see Figure 1). Generally two modules are required, one with pin 1 removed and the second with pin 14 removed, to allow testing of all pins in the socket.

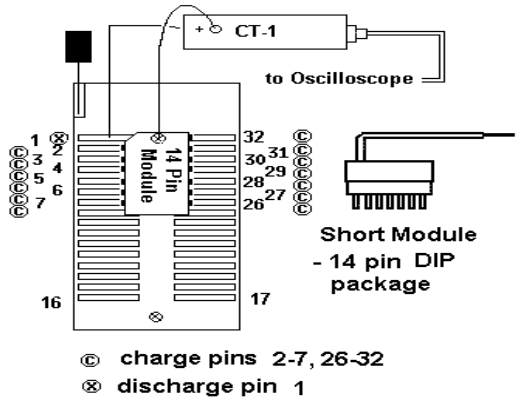

Figure 1: Example of the Short Module placed in a 32-pin socket

NOTE 1: One module can be used, with both pins 1 and 14 removed, however, excessive mechanical stress on the discharge wire placed through the current transformer can cause this wire to detach from the module.

4.2.3 Current Transducer requirements:

4.2.3.1. Minimum bandwidth of 1 GHz.

4.2.3.2. Peak pulse capability of 12 A.

4.2.3.3. Rise time of less than 1 ns.

4.2.3.4. Capable of accepting a solid conductor of 1.5 mm in diameter.

4.2.3.5. Provide an output voltage per mA, usually between one and five mV per mA.

NOTE 2: A Tektronix CT-1 or equivalent with a maximum cable length of 1 m meets these minimum requirements.

4.2.4 Attenuator

4.2.4.1. An attenuator may be used to decrease the signal voltage from the current transducer to the oscilloscope. If a 20-dB attenuator is used, the voltage levels observed will be reduced by a factor of 10 +/- 12% as defined by the manufacturer.

4.2.5 Test Fixture Boards

4.2.5.1. The 32-pin DIP Test Fixture Board is used to verify the waveforms for the 256-pin simulator and the 25x25 PGA Test Fixture Board is used to verify the waveforms for the 512-pin simulator.

5.0 EQUIPMENT CALIBRATION AND VERIFICATION REQUIREMENTS

5.1 Equipment Calibration

5.1.1 Calibrate all equipment used to evaluate the tester periodically in accordance with the manufacturer's recommendation. This includes the oscilloscope and current transducer. Recommended time between calibrations is one year. Calibration shall be traceable to national standards, such as the National Institute of Standards and Technology (NIST) in the United States, or international standards.

5.2 Tester Verification

5.2.1 If the test system uses internal relay matrix switches, then the performance of these relays must be checked. Perform the relay self-test and high voltage test as part of the equipment acceptance testing procedure when the tester is first delivered. Complete the relay self-test and high voltage testing following any repairs or servicing that could affect the discharge waveform. The recommended time between high voltage tests is one year. Retain all waveform records according to the internal record keeping procedures of the organization or institution.

6.0 EQUIPMENT QUALIFICATION AND VERIFICATION PROCEDURES

6.1 Waveform Verification Procedure

6.1.1 Place the wire at the top of the short module through the positive side of the current transducer.

6.1.2 Insert the 14-pin DIP short module into the socket (see Fig. 1), with the wire positioned at either pin 1 or pin 14 of the module, depending on the module being used.

6.1.3 Use the 32-pin DIP for 256 mode or 25x25 PGA Test Fixture Board for 512-pin mode test system configuration.

6.1.4 Insert the 20-dB attenuator into channel one of the oscilloscope, if necessary.

6.1.5 Set-up the oscilloscope for a single shot and with a time scale of 2ns/div. The voltage level is set so that Ip1 can be measured.

6.1.6 If the tester has both, a user control or “manual mode” versus a computer control mode of operation, then set the tester into a manual mode.

6.1.7 Set the charging voltage level to +250V.

6.1.8 Capture a waveform.

6.1.9 Record peak current, Ip1, the rise time, tr, tz and the pulse width, td.

6.1.10 Verify the peak current, rise time and pulse widths are within the verification limits determined in Table 2 (for a 256-pin test fixture board) or Table 3 (for a 512-pin test fixture board).

6.1.11 Repeat steps 6.1.7 to 6.1.10 for a voltage level of –250V.

6.1.12 Repeat steps 6.1.7 to 6.1.10 for +/- 500V, +/- 750V, +/- 1000V and +/- 1250V.

NOTE 3: Refer to Appendix A for procedures to determine Verification Limits.

6.2 Tester Qualification and Re-qualification Procedure

6.2.1 If the test system uses an internal relay matrix switches to change between SDM high voltage and parametric low voltage leakage networks, then the performance of these relays must be checked after any repairs to the equipment have been performed. Test high voltage discharge paths and all associated circuitry according to the equipment manufacturer's procedures (sometimes referred to as Self-Test or VI Test).

6.2.2 The high voltage levels generated by the ESD equipment must be verified. If the equipment has a test point capture location, capture a waveform from the high voltage generator. Refer to the tester manufacturer's manual for detailed procedures.

6.3 Recommended Tester Functionality Check

6.3.1 Test the high voltage discharge path and all associated circuitry at the beginning of each day during which ESD stress testing is performed. Use the tester manufacturer's recommended procedure. If any failure is detected, do not perform testing with the sockets that use the defective discharge paths. Repair and re-qualify the tester in accordance with section 6.2.

6.3.2 Verify the waveform integrity at least once per shift. If necessary, remove the test fixture board being used and replace with the 32-pin DIP for 256 mode or 25x25 PGA test fixture board for 512-pin mode test systems.

6.3.3 Verify the waveform using the short module at +/-1000 V. Longer periods between waveform checks are acceptable if no changes in waveforms are observed for several consecutive checks. However, if the waveforms no longer meet the recommended limits, all ESD stress tests results taken after the last known satisfactory waveform check are invalid.

7.0 SDM TESTING RECOMMENDATIONS

Perform ESD stress testing at room temperature in accordance with the procedure below. Testing can start at any voltage level in Table 1. Additional stress levels to those in Table 1 may be used.

ESD testing should be considered destructive to the component, even if no component failure is detected, and components should not be used for any other application.

7.1 Component Handling

7.1.1 Follow ESD damage prevention procedures whenever handling components before, during, and after testing.

7.2 Component Static and Dynamic Tests

7.2.1 To determine whether components have failed, perform static and dynamic tests to all data sheet parameters before and after ESD testing. Pin leakage current may only be used as a guide to determine the component ESD failure voltage. To use pin leakage as the only criterion for device failure is not sufficient, especially for complex integrated circuits.

7.3 Test Temperature

7.3.1 Stabilize the component at room temperature prior to and during the ESD stress testing period.

7.4 Sample Size

7.4.1 A minimum of three components should be used for SDM testing. Three new components may be used at each voltage level.

7.5 Pin Stressing

7.5.1 Charge the device through the substrate, typically named Vss or Ground pin or through all pins on the device simultaneously.

7.5.2 Discharge through all signal pins, power supply pins (e.g., Vcc) and any peripheral power supply pins (e.g., VSS1, VSSA, VCC1, etc.) in the component, one pin at a time. No Connects (NC) pins are measured as opens and do not need to be stressed.

8.0 SDM ESD STRESS TESTING PROCEDURE

Test a minimum of three samples of the component to all specified static and dynamic data sheet parameters.

8.1 Test Practice

8.1.1 Stress Voltages. Determine the starting stress voltage level from Table 1.

8.1.2 Stress Pulses. Discharge three positive and three negative pulses from the component. The recommended interval between pulses is at least 1 second. Repeat this process for all component pins to be stressed.

8.1.3 Electrical Tests. The components are measured to full static and dynamic data sheet parameters and record the results for each component. Perform parametric and functional testing at room temperature. If testing is required at multiple temperatures, perform testing at the lowest temperature first.

8.1.4 Stress Intervals. If all three components pass the specified data sheet parameters, repeat steps 8.1.2 through 8.1.3 using the next higher stress level of Table 1. Three new components may be used at each voltage level.

8.1.5 Component Failures. If one or more components fail, repeat the ESD stress test using three new components starting at the next lower stress level. If the components continue to fail, decrease the stress voltage until level 1 is reached. If any additional failures are observed at level 1, stop all testing at this level. Lower stress voltages may be applied and smaller stress increments may also be used if the user needs more detailed information.

9.0 FAILURE CRITERIA

A component is considered an ESD failure if it fails the data sheet parameters as specified in sections 7.2.1.

10.0 SDM WAVEFORM PARAMETERS

See Tables 2 & 3 (page 7) for details on the SDM Waveform Parameters (page 7).

Table 1: SDM ESD Stress Levels

Stress Level	Equivalent Charging Voltage (+/-)
1	250V
2	500V
3	750V
4	1000V
5	1250V

Table 2: Average SDM Critical Waveform Parameter values for socket pins (1-32) of a 32-pin DIP Test Fixture Board (256-Pin Test System)

SDM voltage (v)	Ip1 (A) (+/- 20%)	Tr (ps) (+/- 20%)	Tz (ns) (+/- 15%)	Td (ns) (+/- 10%)
250	2.4	700	1.0	4.0
500	4.8	700	1.0	4.0
750	7.2	700	1.0	4.0
1000	9.6	700	1.0	4.0
1250	12.0	700	1.0	4.0

NOTE 4: The peak current will vary as the trace length on the test fixture board changes. The discharge waveform is unique for the 32-pin DIP TFB. Using a different size TFB will produce different waveform parameters including Ip1, tr, tz and td.

Table 3: SDM Waveform Parameters for a 512-Pin Test System

SDM voltage	Ip1 (A)	Tr (ps)	Tz (ns)	Td (ns)
250	1.8	1.0	1.5	10.8
500	3.6	1.0	1.5	10.8
750	5.4	1.0	1.5	10.8
1000	7.2	1.0	1.5	10.8
1250	9.0	1.0	1.5	10.8

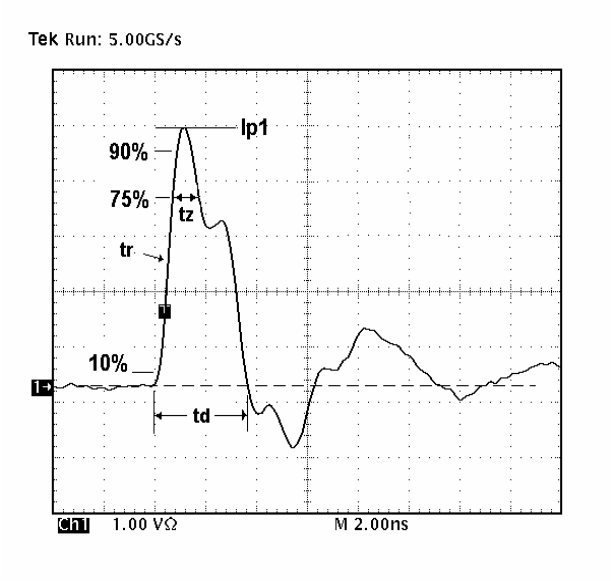

Figure 2: Short module current waveform from a 32-pin DIP Test Fixture Board using a 256-pin test system

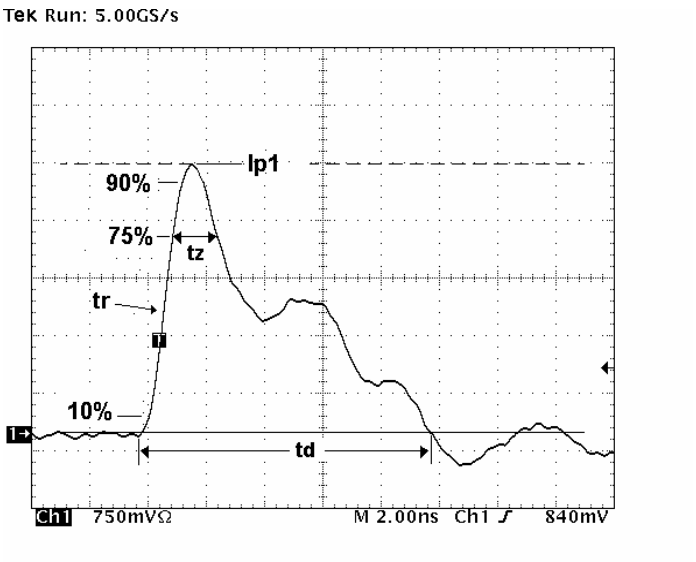

Figure 3: Short module current waveform from a 25x25 PGA 512-pin Test Fixture Board using a 512-pin test system

ANNEX A: WAVEFORM VERIFICATION LIMIT PROCEDURE

The procedure for determining waveform peak current limits is outlined below. The verification limits are dependent on the oscilloscope bandwidth. If an oscilloscope with a different bandwidth is used, the following procedure should be repeated using the new scope. This annex is not part of ESD Association Standard SP5.3.2-2008.

1. Select one socket on the 32-pin dip board to perform the waveform capture.
2. Place the wire at the top of the short module through the positive side of the current transducer.
3. Insert the 14-pin DIP short module device into the socket.
4. Insert the wire from the short module into the socket. Insert the wire into the same socket pin as one of the missing short module pins. Keep the wire as close to the short module as possible.
5. If the tester has either a user control or "manual mode" versus a computer control mode of operation, then set the tester into a manual mode.
6. Set the charging voltage level to (+/-) 1000 V.
7. Set the oscilloscope to a single shot and with a time scale of 2ns/div.
8. Capture a waveform from each pin in the socket.
9. Write down the peak current (Ip1) for each pin in the socket.
10. Calculate the Mean and Standard Deviation of the peak current. Note that most oscilloscopes display voltage levels. To convert to current, divide by the conversion factor listed. For example, the CT-1 Tektronix transducer conversion is 5mV/1mA (e.g., 5V is equivalent to 1A) and a 20 dB attenuator is 10 to 1. The combination of the CT-1 and the 20dB attenuator results in a conversion factor of 0.5V/A.
11. Set the current limits to plus and minus three standard deviations from the mean.

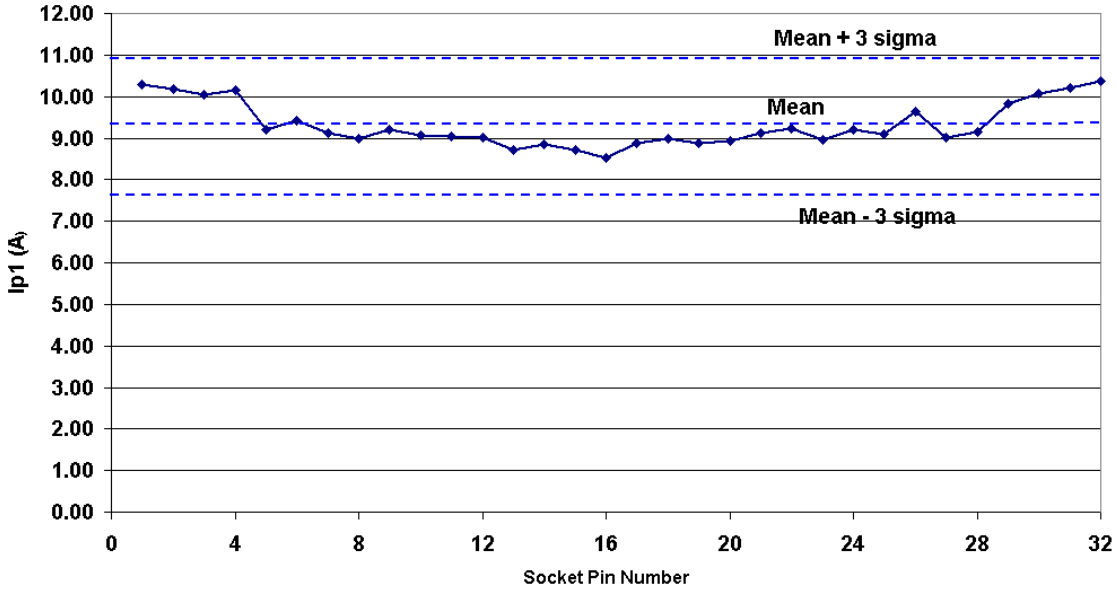

Figure 4: Typical current Ip1 values at 1000V for each pin of a 32-pin DIP TFB

NOTE 5**:** In order to record the waveform from all 32 socket pins two short modules are required. Pin 1 is physically removed from the first module and pin 14 is removed from the second module to allow testing of all pins in the socket. The removal of these pins allows the short module to be placed into all pins in the 32 socket.

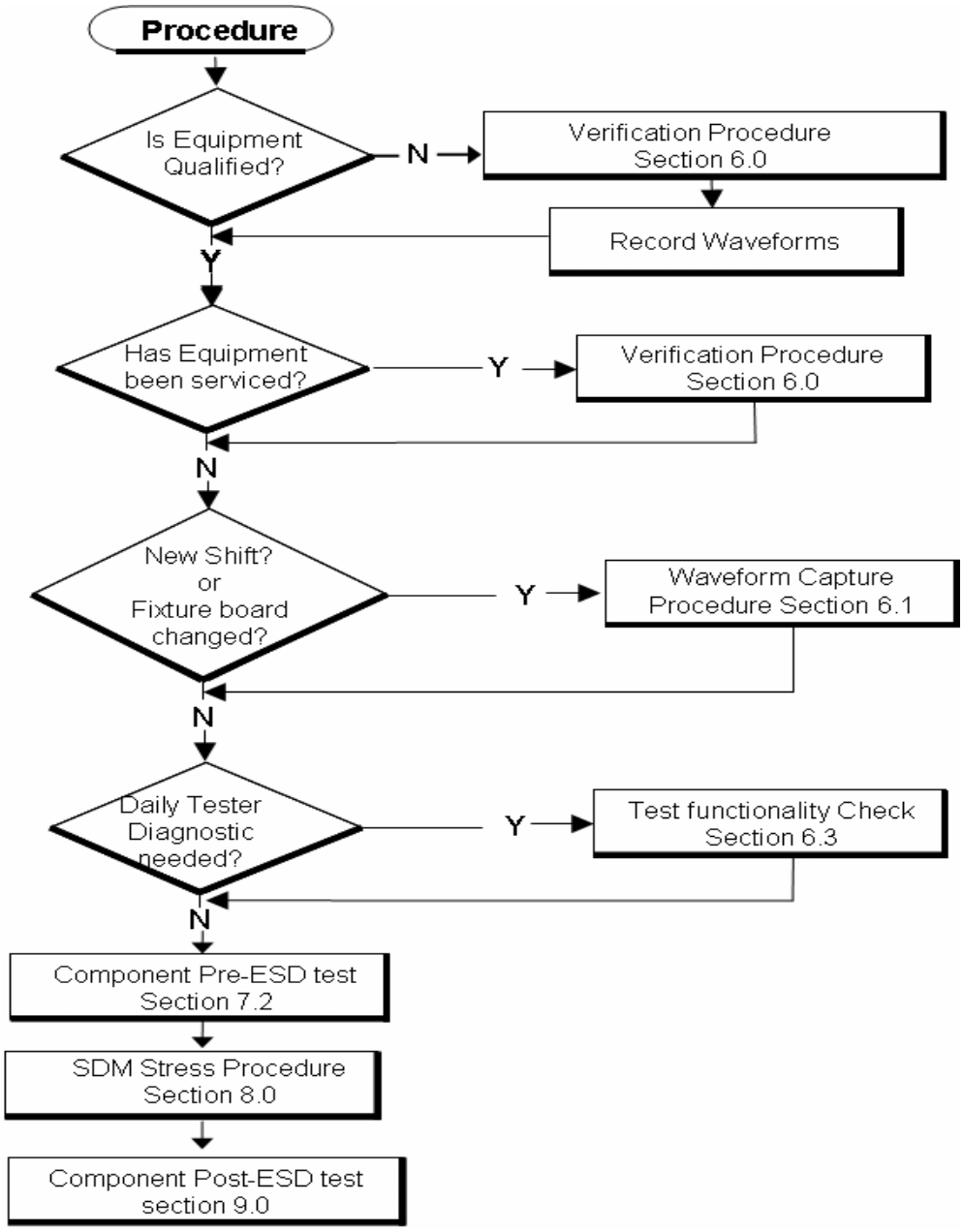

Figure 5: SDM Procedure Flow

THIS PAGE WAS INTENTIONALLY LEFT BLANK

THIS PAGE WAS INTENTIONALLY LEFT BLANK

THIS PAGE WAS INTENTIONALLY LEFT BLANK